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AUTOMATIC INTEGRATED CIRCUIT
TEST SYSTEM.

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THE AUTOMATED DC PARAMETER TESTING OF GaAs MESFETS USING THE SINGER AUTOMATIC INTEGRATED CIRCUIT TEST SYSTEM

THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air Training Command

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science

BY

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Graduate Electrical Engineering

September 1980

PREFACE

This report is in support of the ongoing effort in the fabrication of GaAs MESFET integrated circuits by the Avionics Laboratory, Microelectronics Branch, Air Force Wright Aeronautical Laboratories (AFWAL/AADE). AFWAL/AADE is fabricating GaAs MESFETs in order to establish a baseline GaAs processing capability and requires a knowledge of the DC parameters of the MESFETS. AFWAL/AADE has been obtaining these parameters using a tedious and time consuming manual process. The branch has had the capability to automate this process using available equipment, however, the procedures to perform this process had not been developed. This thesis will attempt to provide the required procedures to automate the data collection process including the results obtained.

I am indebted to the support of Mr. Gordon Rabanus, Branch Chief, Mr. James Skalski, Facility Manager, Mr. Roy Newman, all of AFWAL/AADE, Electronic Technology Division, and my advisor, Major John M. Borky. These gentlemen provided me with valuable technical advice, direction, and support needed to complete this thesis. The effort represented in this thesis is an integration of my two major sequences: Electron Devices, and Digital Computer Systems. I would also like to extend thanks to my readers, Dr. T. E. Luke and Dr. Robert E. Fontana for their support. Additionally, I want to thank Mr. Kevin Pahl and Mr. Newman in the development of the probe cards which were needed to interface the Singer

with the GaAs MESFETs at the wafer level. Dr. Fritz Schuermeyer, Dr. H. P. Singh, Lutz Micheel, Russell Sherer, Ben Carroll, and David Hill provided me with the needed circuit theory and repair of the Singer. Captain J. B. Rawlings, Mr. Andrew Guieterrez, and Mr. Al Carney provided me with the necessary technical information required to operate the Singer tester. Many others were also involved in this technical effort and I would like to extend my thanks and appreciation for their assistance.

My deepest gratitude goes to my parents, Mack and Peggy Harper, and my close friends, Miss Sherry Heath, Mr. Roy Newman and my many friends who provided me continued encouragement and understanding when everything did not seem to be going my way. Without their support and all others previously mentioned, this thesis may not have been completed. Special thanks goes to my typist, Miss Sheri Vogel, for her excellant typing and help when I made thesis format mistakes.

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LIST OF ABBREVIATIONS

ABBREVIATION	DEFINITION
AFWAL/AADE	Air Force Wright-Aeronautical Laboratory, Avionics Laboratory, Micro-Electronics Branch
GaAs	Gallium Arsenide
MESFET	Metal-Semiconductor Field-Effect Transistor
Si	Silicon

NOTATION

AL	Active load MESFET
A_o	Device thickness
BV	Breakdown Voltage at VGS=0
C_{dc}	Dipole layer capacitance
C_{dg}	Drain-gate capacitance
C_{gs}	Gate-to-source capacitance
χ	Affinity of an electron
CS	Current source MESFET
CS1, CS2	Singer current source supplies 1 and 2
CON	Connect
D	MESFET Drain
d	Conductive layer thickness
DGB, DGC	Dual gate MESFET (B and C inputs)
E	Electric field
E_c	Conduction band energy level
ENA	Enable power supply
E_p	Threshold electric field
$\varepsilon_o\varepsilon$	Permittivity
E_W	Energy work function
f_o	Gain-bandwidth product
f_T	Frequency at unity current gain
f_u	Maximum frequency of oscillation
G	MESFET gate
g_m,GM	Transconductance
GND	Ground
I	Current

I_D, ID	Drain current
I_{DSS}, IDSS	Saturated drain current at VGS=0
L_g	Gate length
n	Density of conduction electrons
N_D	Doping density
ω	Frequency in radians
q	Charge of an electron
R_d	Drain resistance
R_g	Gate resistance
α	Specific resistivity of the gate
R_{ON}, RO	"ON" or ohmic resistance
R_{SAT}, RS	Saturation resistance
R_s	Drain-source resistance
S	MESFET source
SF	Source Follower MESFET
SGA	Single gate MESFET (A input)
t_g	MESFET gate thickness
τ_g	Phase delay
V	Voltage
v	Electron drift velocity
V_{Bi}	Built-in voltage
V_c	Voltage drop across source-gate and gate-drain of MESFET
VD	Voltage output of the Single and Dual gates of the MESFET logic gate
VDD	Voltage supply input of the MESFET logic gate

V_{DS},VDS	Drain to source voltage
VF	Forware threshold voltage of a diode
V_G	MESFET gate voltage
V_{GS},VGS	Gate to source voltage
VMH,VML	Voltmeter (high and low connections)
V_P,VP	Pinch-off voltage
v_p	Peak equilibrium velocity
VR	Reverse threshold voltage of a diode
VS1-VS5	Singer voltage sources 1-5
w	MESFET gate width
x	Coordinate in direction of electron drift
y_m	Frequency-independent magnitude (y_m-$g_m e^{-j\omega\tau_o}$)
ZA-ZZ	Varian computer variables
Z_g	MESFET gate width

ABSTRACT

Procedures were developed to automate the manual testing of the DC parameters of GaAs MESFETs, integrated resistors and Schottky diodes. These devices are elements of a NAND/NOR logic circuit developed by Hewlett-Packard. The Singer Automatic Integrated Circuit Test System located at the Air Force Wright Aeronautical Laboratories, Avionics Laboratory (AFWAL/AADE), Wright-Patterson AFB, OH, was used to develop these procedures. The system was built by Singer Aerospace and Marine Systems, Glendale, California to test the DC parameters of semiconductor devices using Singer's Elucidate programming test language.

The following DC parameters for the above devices were to be tested using the Singer tester: drain-to-source voltage (V_{DS}), saturated drain current (I_{DSS}) with gate-to-source voltage (V_{GS}) at 0.0 volts, linear on-resistance and saturation resistance at V_{GS} = 0.0 volts, pinch-off voltage (V_P), transconductance (g_M), breakdown voltage (BV) at V_{GS} = 0.0 volts, diode forward and reverse threshold voltages, and resistance. Test results have been obtained for the following MESFET parameters: V_{DS}, I_{DSS}, V_{CS}, linear on-resistance and saturation resistance, V_p and g_M. Unfortunately, due to system measurement inaccuracies, these results do not compare favorably when compared with curve tracer I-V curves of the MESFETs. This thesis will attempt to demonstrate the feasibility of the Singer to test these parameters given the status of the system.

Additionally, a literature search of several GaAs models has been conducted. A GaAs MESFET model has been proposed from that search that will accurately predict the DC parameter data obtainable on the Singer tester.

I. INTRODUCTION

Background

Within the Air Force, a need exists for a digital processing capability requiring clock rates far exceeding those possible with even the most advanced silicon technology. Requirements projected for 1980 to 1985 are for electronic warfare, telemetry, digital communications, and specialized radar processing systems to cover the 1 to 60 GHz clock-frequency range. Specifically, high speed logic will be required in fast phase-lock loop frequency synthesizers, spread spectrum communications, wideband direct frequency counters, real-time processing of radar data, and high-speed analog-to-digital (A/D) and digital-to-analog (D/A) converters. A 1 to 5 GHz GaAs logic capability can satisfy many of these requirements (Ref 3:1).

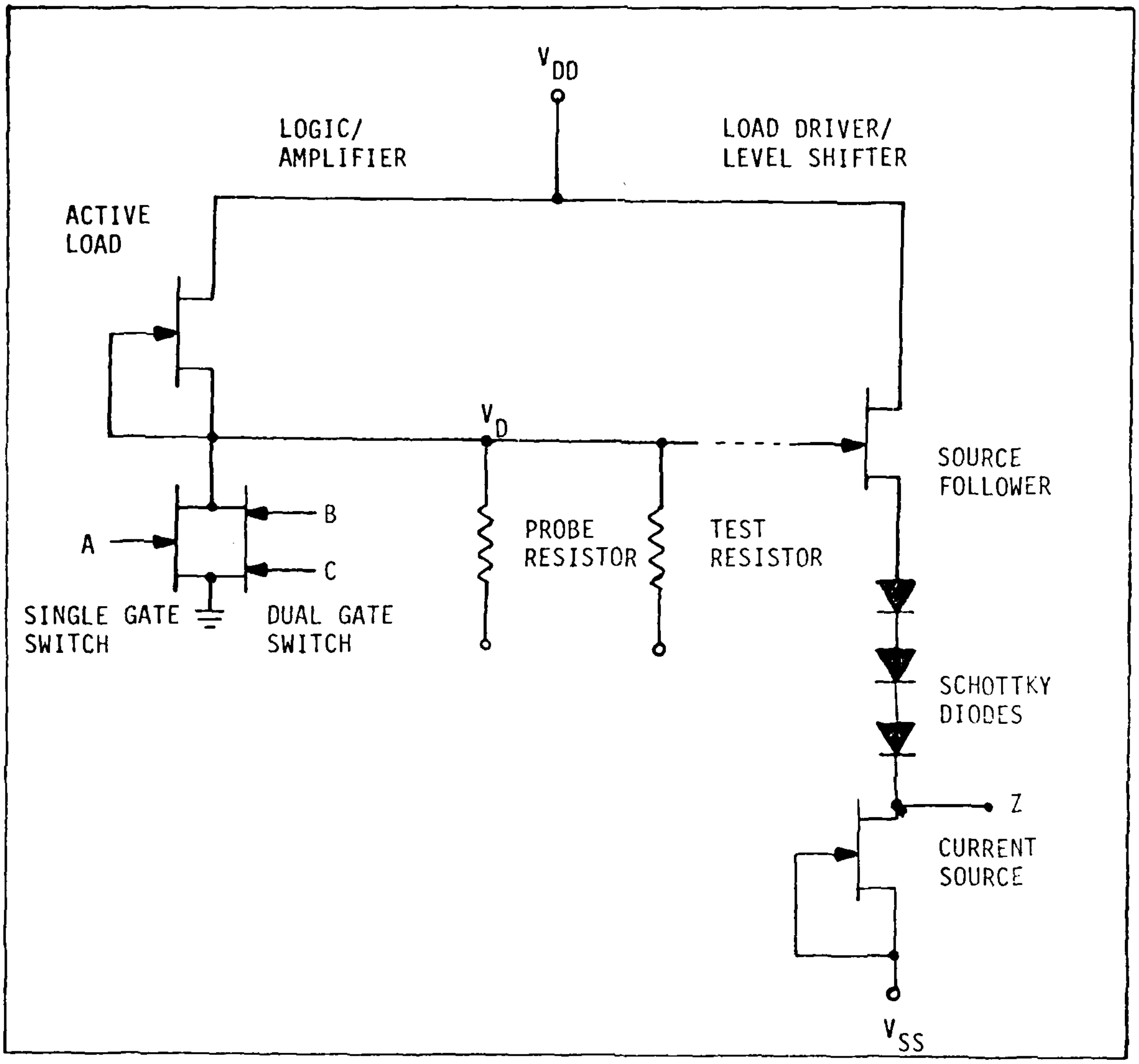
Of particular interest to the Air Force is the GaAs, depletion mode, metal-semiconductor field-effect transistor (MESFET). The GaAs MESFET has been the subject of research and development contracts sponsored by the Air Force Avionics Laboratory of the Air Force Wright Aeronautical Laboratories (AFWAL/AADE) at Wright-Patterson Air Force Base, Ohio. The GaAs MESFET is intended to play a significant role in the future development of the above systems. The specific logic circuits where the GaAs MESFET is expected to play a key role are logic gates, flip-flops, decoders, counters, random access and read-only memories, and, as mentioned previously, A/D and D/A converters.

The GaAs MESFET was chosen by the Air Force for ultra-high-speed digital processing due to its ability to function as a microwave amplifier or subnanosecond switch. In addition, integrated circuits built with GaAs MESFETs are capable of achieving high speed at low power so that medium-scale integration (MSI) circuits can operate at 2-3GHz clock rates (Ref 7:1).

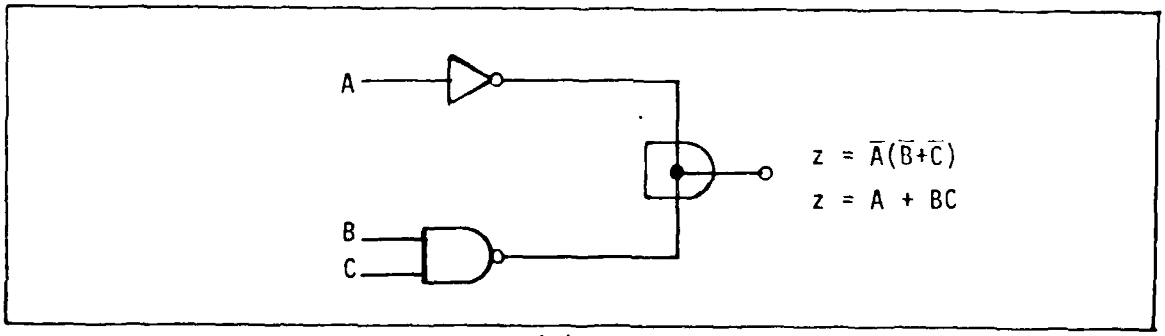
At the present time, AFWAL/AADE is interested in the logic gate as shown in Figure 1(a). The FETs shown in the figure are GaAs MESFETs. Basically, the logic circuit is capable of performing a combined positive logic NAND and positive logic NOR function as can be seen from the expression, $Z = \overline{A}(\overline{B}+\overline{C})$. The device was developed under contract by the Hewlett-Packard Company, HP Laboratories Division, Palo Alto, California several years ago (Ref 4:29). AFWAL/AADE has fabricated this circuit in its own integrated circuit laboratories in order to establish a base-line GaAs processing capability. A problem exists in testing due to the time and effort in obtaining required values of DC parameters for the individual MESFETs. A knowledge of the spread of DC parameters for all MESFETs in a wafer and from wafer to wafer would enable the laboratory to evaluate the fabrication process and identify problems and needed improvements. This ability would eventually contribute to the fabrication of high quality logic gates and the achievement of higher yields.

Current Method Used to Test MESFET Devices

AFWAL/AADE has been studying the DC parameters of the GaAs MESFETs shown in Figure 1 for some time using a manual probing



(a)



(b)

Figure 1. MESFET Logic Gate. (a) Circuit Schematic: (b) Logic Diagram

system. The manual process involves the use of a special probe station, designed specifically for testing individual chips on a 2-inch diameter wafer, and a curve tracer oscilloscope as shown in Figure 48 in Appendix A. The probe station consists of individual probes connected on one end via low resistive wires to the curve tracer while the tip of each probe is placed on a pad on the logic gate. The probe station operator's job is to manually make the proper connections between the chip (Figure 2) and the curve tracer and obtain current-voltage (I-V) characteristic curves that describe the DC operating parameters of a particular chip. This procedure must be performed on each chip with as many as 100 chips or so to a wafer. This manual process takes a considerable amount of time and effort and therefore hinders progress in testing processed wafers. In addition, recording data on each chip through the use of curve tracer pictures and manual data logging complicates the problem even further. Therefore, a special need exists to be able to perform this testing through a more efficient and rapid means.

Statement of the Problem

For the past several years, AFWAL/AADE has had the capability to automatically test devices through the use of a Singer Automated Integrated Circuit Test System. AFWAL/AADE has never before used the system to test FETs. J. F. Skalski of AFWAL/AADE felt that the testing of the GaAs MESFETs' DC parameters could be best performed by its automatic testing system. It was felt that this could provide a more efficient and repid means of obtaining and recording data on the numerous

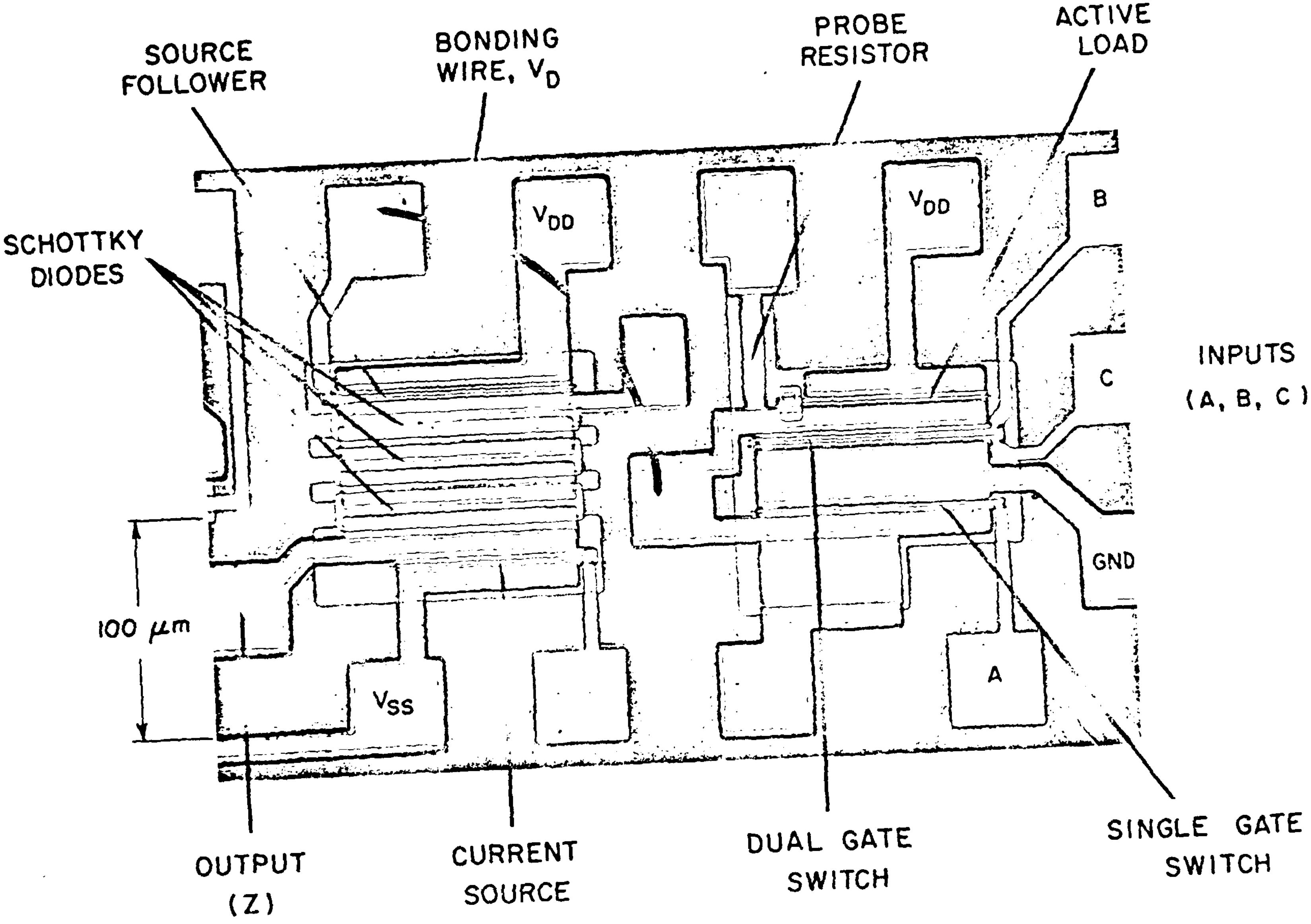


Figure 2. MESFET Logic Gate Chip.

individual chips on a wafer. Therefore, the main goal of this thesis is to develop a more efficient and rapid capability of evaluating and analyzing the static performance and characteristics of GaAs MESFETs of a logic circuit chip as shown in Figures 1 and 2 using the automated system.

The evaluation and analysis consists of developing a computer program to obtain the DC operating parameters of all devices on each chip or die on a wafer. The devices consist of single and dual gate GaAs MESFETs as well as Schottky diodes and resistors as shown in Figures 1 and 2. In addition, all data obtained is to be recorded on magnetic tape for future evaluation and analysis by laboratory personnel. Data retrieval is to be provided using a FORTRAN IV computer program to read data from the tape. The data for the individual MESFETs (by chip) is then to be output to a line printer for subsequent printing.

Programming the Singer tester requires the use of a special test language known as Elucidate. Elucidate is capable of commanding the test system to conduct current, voltage and resistance tests. In other words, static DC testing is the primary specialty of the entire system.

As a second goal of this thesis effort and to provide a further means of analyzing the performance and characteristics of GaAs MESFETs, existing models of FETs are to be studied and evaluated for their suitability for circuit design and testing of these devices. The results of the data obtained through testing are to be used to estimate DC parameters of the appropriate device model in order to provide a quantitative appraisal of the test results and model prediction.

In addition to the above, a study of the existing Singer testing system is to be conducted to determine its capabilities in the area of future high-speed testing.

Scope

This thesis is a culmination of research and analysis of the GaAs MESFET and its use in integrated circuit form. The theory behind the operation of the GaAs MESFET is covered as well as how it is used in integrated circuits. In addition, candidate models of the GaAs MESFET are studied for circuit design and device evaluation. The DC operating parameter results are presented, analyzed, and used to validate the model chosen to depict these parameters. Also, test programs to automatically test GaAs MESFET's on the wafer are presented including an analysis of the results obtained. Finally, the capabilities of the testing system are evaluated.

Assumptions

Much of the underlying theory of the DC parameters of the depletion mode, n-channel junction field-effect transistor (JFET) can be applied to the depletion mode, n-channel MESFET. This is explained further at the beginning of Chapter II. Therefore, it has been assumed that much of this theory can be accepted without proof since it is used in many research articles and is accepted throughout the field of micro-electronics and semiconductor device physics. All equations and ideas are, of course, referenced so as to insure credibility.

Approach

The general approach taken in the thesis is to present the theory behind the operation, and the characteristics of, the GaAs MESFET. From here, a study of the GaAs MESFET's use in an integrated circuit is covered as well as the operation of the circuit as a whole. Tests performed and results obtained using manual testing are discussed. These results are then applied to the model of a GaAs MESFET (single-gate) to determine their suitability for DC parameter modeling. A model of the dual-gate, taken as the combination of two single-gate MESFETs in cascade, is proposed and discussed. In addition, the basics of the Singer Automated Testing System are presented as well as the computer program and results obtained from testing a single-gate MESFET. The capabilities of the system are then discussed.

Sequence of Presentation

In Chapter II, a study of the theory behind the operation of the GaAs MESFET, as well as its static, high-speed and low power characteristics are presented. The use of the GaAs MESFET in a logic circuit is discussed, included design consideration, using NAND/NOR logic circuit, Figure 1(a), as an example.

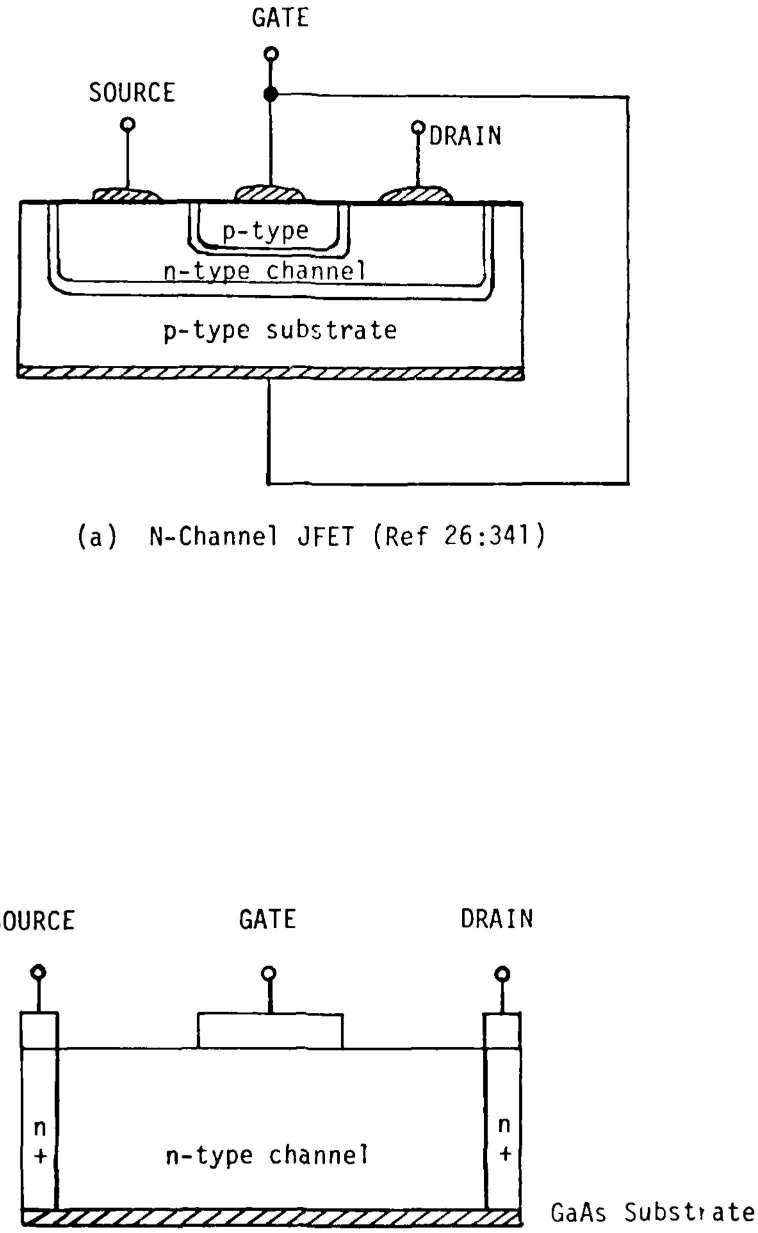
The proposed models of the GaAs MESFET single-and dual-gate models are presented in Chapter III. A study of each of these models is made as well as an analysis of the single-gate model's potential in simulating or modeling its DC parameter characteristics. DC parameters were obtained from a MESFET tested manually as presented in Appendix A.

Procedures, algorithms, and flowcharts used to present the development of the MESFET program that automatically tests the DC parameters of the devices in Figure 1(a) are presented in Chapter IV. In Chapter V, the results obtained from automatically testing the DC parameters of the devices in Figure 1(a) are presented.

In Chapter VI, a brief capability and limitation study of the Singer tester is presented. A conclusion outlining accomplishments of the thesis project as well as recommendations which might lead to further investigation and development in the automated testing of the GaAs MESFET are presented in Chapter VII.

II. GaAs MESFET AND SCHOTTKY BARRIER DIODE THEORY

The GaAs metal-semiconductor field-effect transistor (MESFET) exhibits current-voltage characteristics as well as operating DC parameters very similar in most respects to junction field-effect transistors (JFETs). This is due to the fact that both are three-terminal semiconductor devices in which the laterial current flow is controlled by an externally applied vertical electric field. According to Schockley, the JFET is a unipolar transistor because the current flow is carried by one type of carrier only, the majority carrier (Ref 2:1365). The MESFET can also be considered to be unipolar transistor since current flow is also due to majority carriers, specifically electrons (Ref 1:319). Both devices are characterized by a lightly doped active channel region between two heavily doped gate regions. The channel current flows between the drain and source terminals which are formed by ohmic contacts (Ref 9;182 and Ref 6:285). (See Figure 3.) There are, of course, several differences between the GaAs MESFET, and, say, a silicon JFET. For instance, the high speed and power capabilities, and the drift velocity vs. electric field characteristics are different in each device, but these will not be elaborated upon. There is one structural difference worth briefly mentioning. The difference lies basically in the gate regions. In the JFET, the gate terminal is formed by a p+ region for an n-type channel. In the MESFET, the gate is formed by a metal-to-semiconductor (n-type) contact known as a Schottky barrier.



(a) N-Channel JFET (Ref 26:341)

(b) N-Channel GaAs MESFET (Ref 30:287)

Figure 3. Cross-Sections of an N-Channel JFET and GaAs MESFET.

MESFET Theory of Operation

As in the JFET, the MESFET is basically a 3-terminal device consisting of the source, drain, and gate. Figure 4(a) is a simple view of an n-channel, depletion mode GaAs MESFET, exluding the gate. A depletion mode MESFET implies that substantial drain current flows when the gate is shorted for zero gate bias (Ref 13:197).

The majority carriers, in this case electrons, enter the MESFET through the source(S) contact and leave the MESFET through the drain (D) contact. The electrons flow from source to drain with a velocity determined by the applied forward bias from drain to source. Current flow is proportional to the applied drain to source voltage, V_{DS}, at low voltages and therefore the MESFET behaves like a linear resistor (Ref 6:285). The current flow, however, departs from linearity at larger voltages due to the fact that the electron drift velocity reaches a peak value at about 3kv/cm, and then decreases and levels off at a saturated velocity slightly higher than in silicon, as shown in Figure 5. The saturation velocity in GaAs differs by no more than 10 percent from the value obtained in silicon (Ref 25:652). However, the gain-bandwidth product of the FET, f_o, could rise to as much as 30 GHz if GaAs is used instead of Si due to the larger saturation drift velocity in GaAs (Ref 10:93). (The current-coltage curve therefore falls below the initial resistor line and the current begins to saturate as shown in Figure 5 (L_g = gate length > 3μm.)

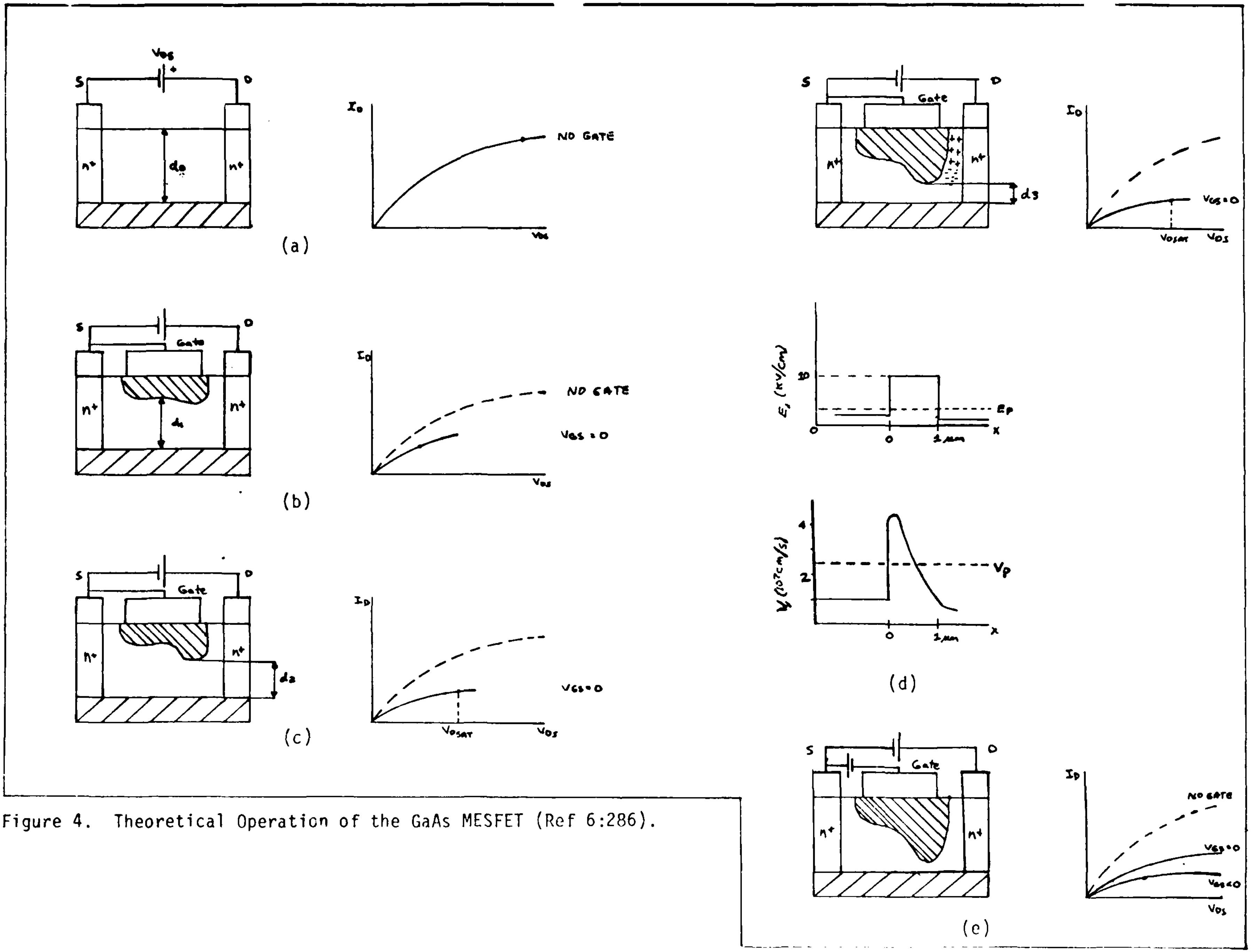


Figure 4. Theoretical Operation of the GaAs MESFET (Ref 6:286).

Between the source and drain, a metal-to-semiconductor contact (or Schottky barrier) known as the gate has been added as shown in Figure 4(b). The gate creates a layer in the semiconductor that is depleted of free-carrier electrons. This depletion region acts somewhat like an insulator that constricts the current flow in the channel. The depletion region width depends on the voltage applied between the source and the gate, V_{GS}. In Figure 4(b), the gate is shorted to the source ($V_{GS} = 0$) and a small drain voltage is applied. As a result, the depletion region has a small width and the conductive channel below has a smaller cross section d_1 than d_0 in Figure 4(a). Therefore, the resistance between the source and drain is larger. The saturated drain current is given by

$$I_D = qwn(x)d(x)v(x) \tag{1}$$

As long as $E>E_p$, the electron density n is equal to the constant donor density, N_D (equilibrium). Voltage in the channel is zero at the source and increases along the channel to the applied V_{DS} at the drain. The depletion region becomes wider from the source to the drain and the gate becomes increasingly reversed biased as shown in Figure 4(c). A constant current through the channel is therefore maintained as a result of the decrease in conductive cross section d_2.

In GaAs MESFETs with very short gate lengths ($L_g > 3\mu m$), conditions in the high-field region of the channel are not the same. As long as E is maintained below the threshold field, E_p, the electrons remain in equilibrium (Figure 4(d)).

At about $E=E_p$, and where $d_3=d_1$, to preserve current continuity according to (1), a heavy electron accumulation layer must form in this region because the channel cross-section is narrowing. If the electrons enter a high-field region ($E>E_p$), they are accelerated to a higher velocity before relaxing to the equilibrium velocity. As shown in Figure 4(d), the peak equilibrium velocity, v_p, is doubled for $E>E_p$. The doubling of the electron velocity shortens the electron transit time through the high-field region and at the same time shifts the accumulation layer between the gate and drain.

In Figure 4(e), with a negative voltage applied to the gate, the gate-to-channel barrier becomes reverse biased, and the depletion region grows wider. The channel acts as a linear resistor as before for small values of V_{DS}. However, the channel resistance will be larger due to a narrower cross section and hense a small current flow. For further increments of V_{DS}, E_p is reached at a lower drain current than in the $V_{GS} = 0$ case. The current remains saturated for a further increase in V_{DS} (Ref 6: 285-288).

MESFET Static Characteristics

The n-channel MESFET is summarized in Figure 4. For an n-channel MESFET, the gate is reverse biased as shown to form a depletion region under the gate. The MESFET is connected in the common-source configuration with the drain to source forward biased as shown. The common-source drain characteristics for an n-channel MESFET are shown in Figure 6, a plot of I_D verses V_{DS}, with V_{GS} as a parameter. The characteristics can be explained with $V_{GS} = 0$. The channel is completely open when $I_D = 0$. For a small applied voltage V_{DS}, the MESFET acts as a simple semiconductor resistor whereby the current I_D increases linearly with V_{DS}. While the current is increasing, the ohmic voltage drop between the source and the channel reverse-biases the junction, and eventually the channel begins to constrict. The constriction is not uniform because of the ohmic drop along the length of the channel itself. The constriction is more significant near the gate and drain as shown in Figure 4(d). Finally, a voltage V_{DS} is reached at which the channel reaches "pinch-off". This is the voltage where the current I_D levels off and approaches a constant value. In principle it is not possible for the channel to close completely and therefore reduce I_D to 0. Each value of V_{GS} produces a characteristic curve with an ohmic region for small values of V_{DS} and a constant-current region for large values of V_{DS} where I_D responds only slightly to V_{DS}.

With a gate voltage V_{GS} applied in the direction to provide further reverse bias, pinch-off will occur for smaller values of V_{DS}, with the maximum drain current even smaller. This can be seen in Figure 6.

The maximum voltage that can be applied between any two terminals of the MESFET is the lowest voltage that will cause avalanche breakdown across the gate junction. As shown in Figure 6, avalanche breakdown occurs at a lower value of V_{DS} when the gate is reverse-biased than for

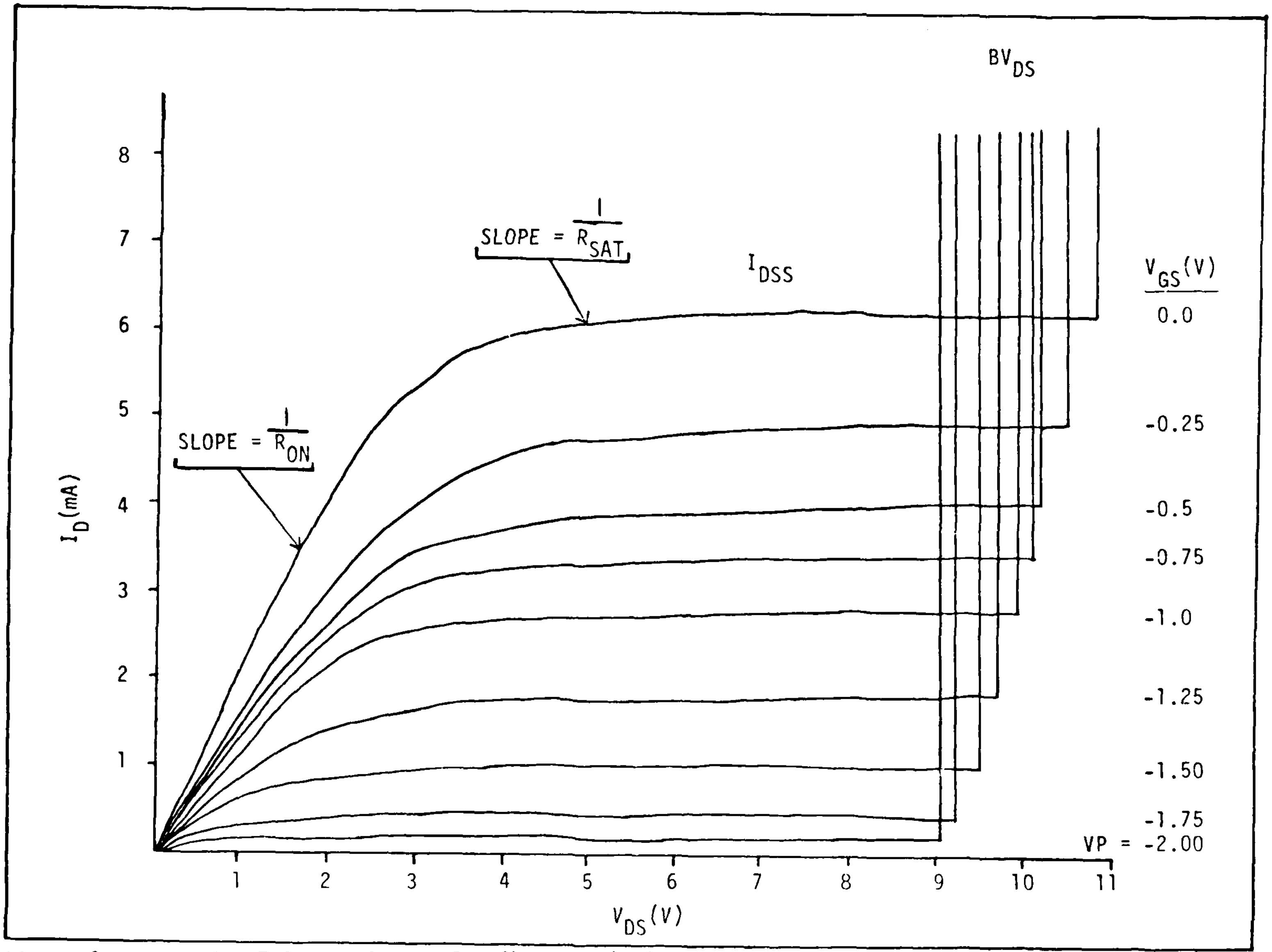


Figure 6. GaAs MESFET Common-Source I-V Characteristics.

$V_{GS} = 0$. This is due to the fact that the reverse-bias gate voltage adds to the drain voltage, and thereby increases the effective voltage across the junction (Ref 11:312-214).

Important DC Parameters

Typical values of DC operating DC parameters that describe the switching operation for n-channel GaAs MESFETs with 1μm x 500μm gates are:

I_{DSS}	75ma
$I_D(max)$	120ma
V_p	-2.5V
R_{ON}	850 ohms
g_m at $V_{GS} = 0$	50 mmho
$V_{GS}(max)$	0.8V
R_{SAT}	2000 ohms
Breakdown Voltage (at $V_{GS} = 0.0V$)	10V

(Ref 4:4-6)

The theory and the techniques underlying measurement of the listed DC parameters will now be presented.

Drain current, designated by I_D, is given by

$$I_D = I_{DSS}\left(1- \frac{V_{GS}}{V_p}\right)^2 \qquad (2)$$

where I_{DSS} is the saturated drain current with the gate shorted to the source ($V_{GS} = 0$), V_{GS} is the gate-to-source voltage, and V_p the pinch-off voltage. Equation (2) is the transfer characteristic of the MESFET in saturation given the relationship between I_D and V_{GS} and is parabolic as shown in Figure 7. I_D can be found (through actual measurement) by simply measuring the current entering the drain from a power supply voltage (V_{DS}) using a milliammeter inserted in series. A reverse-bias voltage is then applied between the gate and source, V_{GS}. I_{DSS} can be measured in the same manner with $V_{GS} = 0$ or the gate and source shorted. By varying V_{DS} at a certain applied V_{GS}, the characteristic volt-ampere curves can be obtained as in Figure 6 (Ref 4:5).

The pinch-off voltage, V_p, is used to describe the value of gate-to-source voltage, V_{GS}, that will "pinch-off" or constrict the channel and thereby reduce the drain current, I_D, to approximately zero (Ref 11:313). V_p can be found by measuring I_{DSS} (at $V_{GS} = 0$), taking 1% of that value of drain current, and then increasing V_{GS} in the negative direction while monitoring the drain current. When the drain current is approximately equal to 1% of I_{DSS}, that value of V_{GS} at the time is taken as V_p. The pinch-off voltage is shown in Figure 6 (Ref 12:82).

The MESFET behaves like an ohmic resistance for values of V_{DS} well below saturation. The "ON" drain resistance, R_{ON}, is the ohmic resistance and is found by the ratio V_{DS}/I_D at a given applied V_{DS}. R_{ON} is simply the reciprocal of the slope in the region prior to saturation for a specific V_{GS} as shown in Figure 6 (Ref 11:316).

The mutual conductance or transconductance of a MESFET is an important forward transfer characteristic. It is an expression that indicates how much change in output current may be induced by a change in the input voltage,

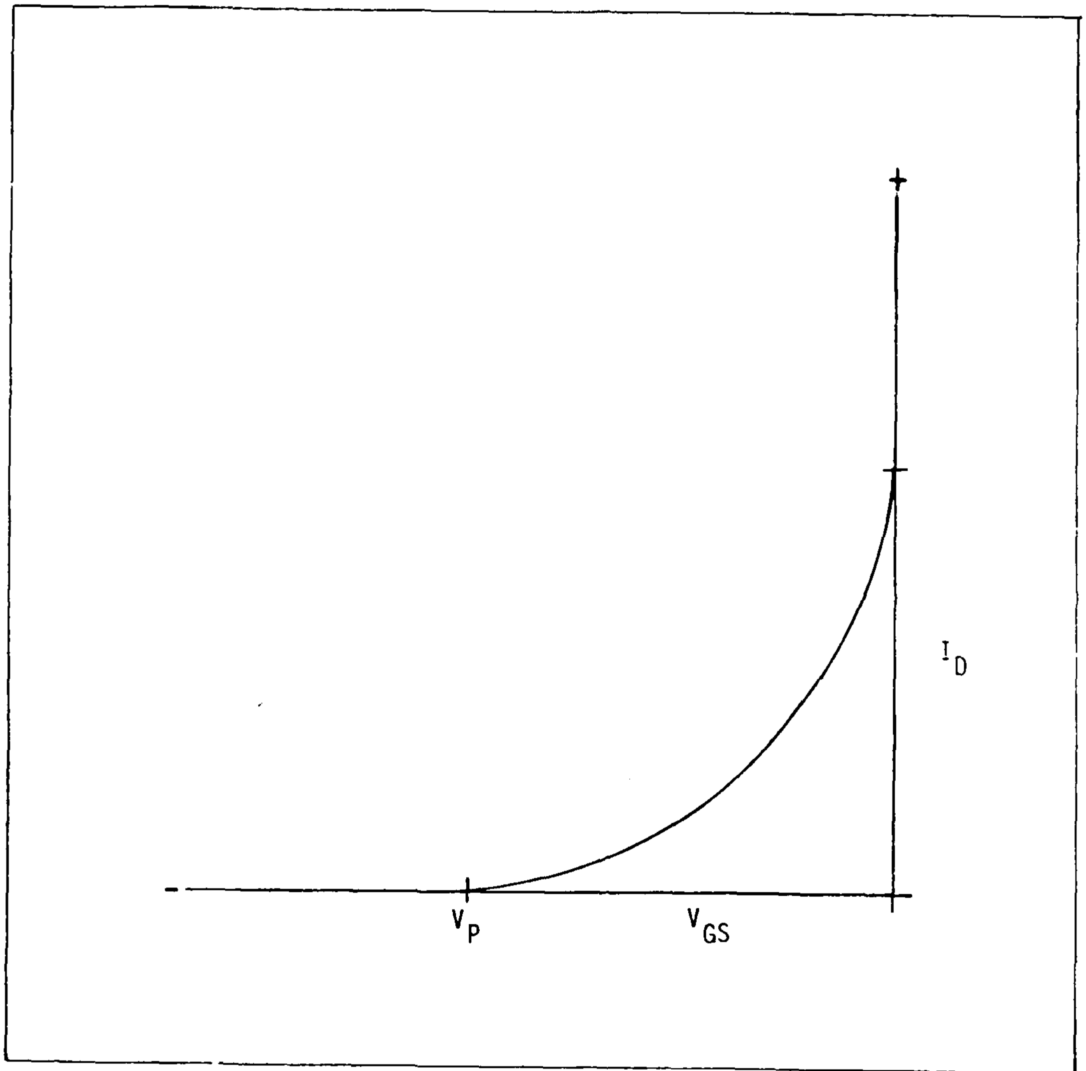


Figure 7. MESFET Transfer Characteristic (Ref 11:337).

i.e., the basic gain of the device, and is given by

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \text{, at a given } V_{DS}. \tag{3}$$

Transconductance can be determined from Figure 6 by setting V_{DS} at a specific value and then taking two values of I_{DS} at two different values of V_{GS} and applying these to equation (3) (Ref 12:86).

The resistance of the channel in the saturation region is the output resistance, R_{SAT}, and is taken as the reciprocal of the slope in the saturation region (for an applied V_{GS}) as shown in Figure 6. The output resistance is given by the ratio $\Delta V_{DS}/\Delta I_D$ in the saturation region for a given V_{GS} (Ref 15:163).

High-Speed and Low-Power Characteristics

The power consumption of any high speed logic device must be no higher than necessary to achieve its speed objectives. Monolithic integrated circuits built with GaAs MESFETs can achieve high switching speed at low enough power for medium-scale-integration (MSI) circuits to operate at multi-gigahertz clock rates (Ref 7:41). According to Liechti (Ref 14:489), MSI packing densities require a power consumption of less than 50 MW per gate for a total power dissipation of 1 watt or less for an entire chip. In order to lower the circuit-power, it is necessary to decrease the gate width of the MESFET. This, however, increases the propagation delay and therefore reduces the high-speed capabilities of the circuit. In other words, propagation delay is inversely proportional to power. For example, a NAND/NOR GaAs MESFET logic circuit with 10µm gates has been experimentally determined by Liechti (Ref 14:490) to have a propagation delay of 142 ps and a power consumption of 20mW per MESFET. For 20µm gate widths, a propagation delay of 111 ps and power consumption of 40 mW per MESFET has been determined.

An approach to explain the high-speed and low power characteristics of the GaAs MESFET can be made using semiconductor device physics and comparing GaAs with Si. In GaAs, electrons have six times higher low-field mobility than in silicon doped to the same level with n-type impurities as shown in Figure 8. This results in lower operating voltages and lower 'ON' resistances for switching applications, and thereby reduces power consumption. The maximuj electron velocity of GaAs is about twice that of Si as shown in Figure 5. This results in a larger current change for a given gate voltage change (higher g_m(, and therefore enhances switching speed (Ref 7:42). The saturation velocity for GaAs is slightly higher than Si. As a result, the current-gain bandwidth, f_T, is about two times higher and the maximum frequency of oscillation, f_u, is three times higher in GaAs as opposed to Si (Ref 5:289).

To achieve the highest possible switching speed, the metal-semiconductor gate electrode, which forms a rectifying Schottky barrier contact, must be very narrow-about 1µm (Schottky barrier gate length) in today's technology (Ref 7:42). Decreasing the gate length (L_g) decreases the parasitic gate-to-source capacitance, C_{gs}, and also increases the transconductance,

g_m. As a result, f_T is improved. For short gate length MESFETs f_T is proportional to $1/L_g$ (Ref 6:289).

Schottky Barrier Gate Theory

The Schottky barrier gate metalization, as shown in Figure 3, consists of evaporated chromium, platinum, and gold (Ref 3:19). The gate is 1µm in length and 600µm in width forming a metal n-type semiconductor contact for outside connections (Ref 4:4).

According to semiconductor device physics, when a metal makes contact with a semiconductor, the Fermi levels on both sides align themselves after some charge movement. The Fermi level in metal falls inside the conduction band and can be looked upon as the average energy of the most energetic electrons in the metal. For an energetic electron to be completely emitted from the metal to the outside, a minimum energy, E_W (Metal), known as the work function of the specific metal, must be added above the E_F of the metal.

As in a metal, some minimum energy msut be added in a semiconductor to get electronic emission. However, since E_F is located in the forbidden gap where electrons in the semiconductor cannot possess energies between the conduction and valence bands, a quantity called affinity and denoted by χ is also used. Affinity is the additional energy that an electron at the bottom of the conduction band, E_C, must have to be emitted. This is shown in Figure 9(a) (Ref 16:107).

As shown in Figure 9(b), when a metal makes contact with a semiconductor of a different work function, the two Fermi levels align in equilibrium after a momentary shift of electrons from the material with the smaller work function to that with the higher which reduces free energy. Fermi-level alignment is reached when an electric potential difference has built up at the interface between the two materials equal to the difference between their work functions. This situation after contact is shown in Figure 9(b) where n-type semiconductor is contacted by a metal of a higher work function.

Electrons pass from the semiconductor into the metal since the metal has a higher work function than the semiconductor. The loss of electrons creates a positively charged depletion region in the semiconductor near the interface between the metal and the semiconductor. The depletion region extends into the semiconductor for a depth depending on the doping density which is much lower than the allowed states and electron densities in metal around E_F. The shift of E_F in the metal will be small while the shift and band banding in the semiconductor will take up practically all the potential difference given by E_W (Metal) - E_W (Semicon.). Once this potential difference has grown to $[E_W(\text{Metal})-E_W(\text{semicon.})]/,9$, equilibrium is reached, the depletion region is stabilized, and no further net charge will cross the junction (Ref 16: 107-108).

A large density of surface states will always be found at the crystal discontinunity of the surface of the semiconductor material. These states will cause band bending without making contact with metal. After contact with metal, the surface

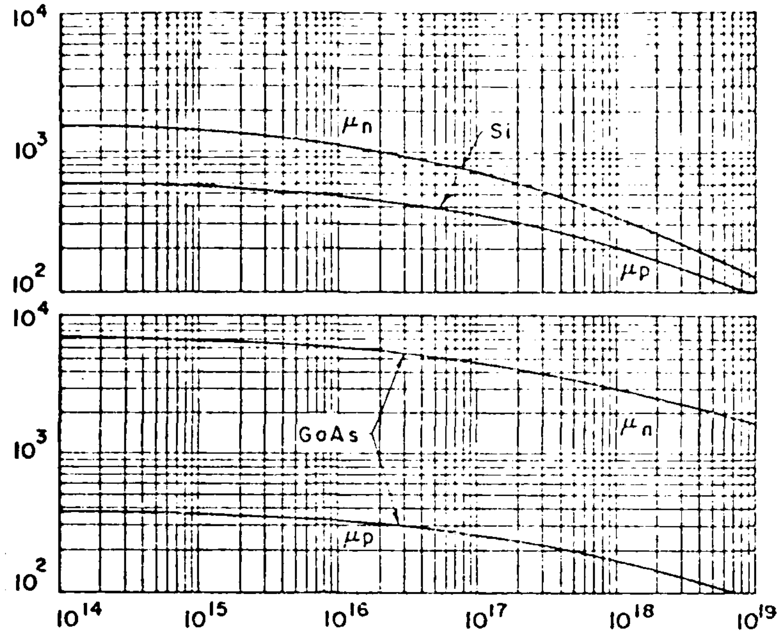


Figure 8. Drift Mobility of Silicon and Hall Mobility of GaAs at 300°K vs. Impurity Concentration. (Ref 17:40).

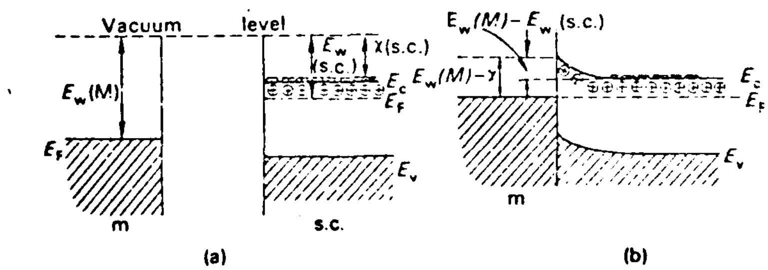


Figure 9. Metal to n-type Semiconductor Contact when $E_W(m) > E_W$ (Semiconductor). (hatched areas represent electron-filled energy levels: (a) Before Contact; (b) After Contact) (Ref 16:107)

states reduce the effect of a particular metal work function on the band banding (Ref 16:109-110).

GaAs MESFET NAND/NOR Logic Circuit Design Considerations

The GaAs MESFET is a very fast switching transistor capable of converting a voltage change at its gate electrode into a drain-current change in about 10ps (propagation delay). The drain-current change must then be capable of developing a voltage change suitable for driving the input of another MESFET. This current-to-voltage conversion is the cause of much of the delay in a MESFET logic circuit due to the circuit capacitances that must be charged (Ref 7:42). It now becomes necessary to further discuss the use of the GaAs MESFET in an integrated circuit as well as required design considerations using Figure 1(a) as an example.

Figure 1(a) is capable of performing a combined positive logic NAND, and a positive logic NOR function as can be seen from the expression $Z = \overline{A}(\overline{B} + \overline{C})$ (Ref 4:29). The NAND/NOR logic gate exhibits a 100-ps propagation delay at 400mW power consumption yielding a 4-pJ speed-power product (Ref 14:495) and responds to clock rates from 0 to 4GHz (Ref 7:41). The logic diagram for the circuit is shown in Figure 1(b).

The logic gate uses parallel switching in the form of the two input MESFETs, as well as series switching, in the form of the dual-gate input transistor (inputs B and C) (Ref 4:29). The current-sourcing level in the circuit is a high impedance active load with the gate connected to the source (Ref 5:21). The active load of the circuit provides a high gain (Ref 5:21) minimizes power dissipation (Ref 4:28) and is somewhat invariant to device parameter changes (Ref 5:21). The high impedance node located between the active load and switch is highly susceptible to capacitive loading. It is for this reason that a buffer circuit must be incorporated into the logic gate to provide a low output impedance which is insensitive to capacitive loading (Ref 5:21, 24).

Since the MESFET is a depletion mode device, there is an incompatibility between the input and output (Ref 7:42). A level shift is required to make the input and output voltage levels of the logic circuit compatible. This level shift is provided by using Schottky diodes in the output buffer circuit. The number of diodes required is determined by the pinchoff voltage of the MESFET and in turn determines the magnitude of the logic swing (Ref 5:24). In this circuit, three diodes are used, each with a forward threshold voltage of about 0.8V. The series voltage drops total 2.4V thus assuming that the MESFETs should pinch-off at no more than -2.4V. The source follower, which is incorporated into the level shifter/ buffer circuit, provides extra current for driving capacitance loading. Current is drawn through the constant-current source, thereby producing a voltage drop across the three series-connected Schottky diodes. The output at 2 will now be compatible to meet the input requirements of another MESFET logic gate.

Theory of Operation. The study of the operation of the circuit of Figure 1 will be conducted by treating it as a logic gate that switches DC level inputs only. The switching time and frequency response of the circuit will not be covered since this thesis is primarily centered around the study of DC parameters.

The heart of the MESFET logic gate consists of the single-gate (A input) and the dual-gate (B and C inputs) as shown in Figure 1(a). These gates and their respective inputs determine the output, z, according to Table I. A logic 0 applied at the inputs will pinch off or turn off the MESFETs and, ideally, an open circuit will result. An applied logic 1 will turn the MESFETs on and they will represent a small resistance with a voltage drop. The logic gate uses positive logic whereby a logic 0 represents -2.4 volts, and a logic 1

TABLE I. Truth Table for the GaAs MESFET Logic Gate of Figure 1.

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

represents 0.5 volts. For A=0, and B=C=0, or if either B or C = 1, current is drawn from the active load below its saturation point, and node 1 will be high. For A = 0, and B=C=1, current is drawn from the active load beyond the saturation point. The depletion region area of the active load has decreased toward the source and therefore the channel resistance has increased toward the source. Therefore, the voltage drop at node 1 has reached to a logic 0. Similar explanations can be given for the remainder of the table.

At node 1, a logic 0 will be about 0.5V and a logic 1 will be about 4.0V. Since, and in keeping with positive logic, the lowest voltage input is assumed to be a logic 0 and the highest a logic 1. In addition, the levels have changed to an incompatibility between the input and output since the MESFETs are depletion mode devices. The inputs will be brought to their proper levels after they are applied to the level shifter as brought out in the previous section. The output will be shifted to its proper level as shown in Figure 1(a) so that it will meet the input requirements of another MESFET logic gate connected in cascade.

Summary

In this chapter, MESFET device theory was presented. The emphasis was placed on the static operation of the MESFET to provide a foundation for the modeling effort and automated testing. Models for the single and dual gates of Figure 1(a) will now be proposed and disucssed in Chapter III.

III. PROPOSED MODELS OF THE SINGLE GATE AND DUAL GATE GaAs MESFETs

AFWAL/AADE is currently conducting efforts in the modeling of GaAs MESFETs. The modeling effort will aid in understanding the static and dynamic behavior of MESFETs currently fabricated by AFWAL/AADE as well as any possible MESFET Circuit design efforts. To aid in this effort, a study of the static characteristics only will be conducted in this chapter. A literature search of the efforts conducted by a few leading professionals in the field of GaAs MESFET modeling will provide AFWAL/AADE with references for further study. The search will be presented following a presentation of criteria to be used in the evaluation and subsequent selection of models for the GaAs dual and single gate MESFETs. Selected models studied in the literature will be subjected to the criteria. A single gate and dual gate model will be finally proposed after a study of the elements used to model the DC parameters is conducted. The proposed single gate model will be analyzed further in order to determine its accuracy in predicting DC parameter data that could be obtained on the Singer tester.

Criteria Established for the Selection of the GaAs MESFET Models

The following are the criteria used in the evaluation and subsequent selection of the GaAs MESFET model used in conjunction with device measurement and characterization in this thesis:

1. The model must be suitable and convenient for use in digital integrated circuit design by accurately modeling the DC parameters of the MESFET and by being computationally tractable in circuit design and analysis.

2. The model must be appropriate for evaluation and prediction of DC parameter data to be eventually obtained from the Singer tester.

An evaluation of the above criteria is in order at this time. In the testing of DC parameters of the MESFET, it is important to know where pinch-off may occur or the point where the MESFET switches on or off. The rate at which this occurs is dependent on frequency. Since the dynamics of the MESFET are not emphasized in this thesis, the rate will be ignored. The emphasis lies in whether the MESFET reaches pinch-off and if so at what point. Therefore, the MESFET will be modeled with its use as an element in a digital integrated circuit kept in mind.

Obtaining a suitable model will aid in predicting the MESFET's DC parameters in a convenient manner and thus give direction to device testing. These parameters would be derived from points found on a MESFET's characteristic I-V curves. The model would actually consist of a network of circuit elements which simulates MESFET behavior under actual DC conditions and yields the values found in the measured I-V curves. These model parameters would be calculated from the curves. The DC parameters that will be obtained from the Singer tester and used to model the DC conditions of the MESFETs later in the chapter are the following:

1. Drain Current, I_D
2. Gate to Source Voltage, V_{GS}
3. Saturated Drain Current, I_{DSS}
4. Linear On-Resistance, R_o
5. Saturation Resistance, R_s
6. Pinch-Off Voltage, V_p
7. Transconductance, g_m
8. Drain to Source Voltage, V_{DS}

The model to be eventually proposed and analyzed should be able to be used to model I_D, V_{GS}. R_o, R_s, and G_m as equivalent circuit elements. I_{DSS} and V_p are parameters required to determine I_D and do not vary for a particular MESFET. V_{DS}, and I_D are used to determine R_o, and R_s, whereas, I_D, and V_{GS} are used to determine g_m. This will be pointed out in the element defining equations presented in the chapter.

Literature Search

A literature search was conducted to determine the GaAs MESFET models available. Numerous models of the single gate device were studied. The purpose of this section will be to present a few of the models studied that were developed by several leading professionals and a brief description of each.

Single Gate Model. Liechti (Ref 6:288) modeled the GaAs MESFET as an RF equivalent circuit with the MESFET channel modeled as a distributed RC network. The model was developed for operation in the saturated current region in a common-source configuration. Liechti also studied the high-frequency limitations of the MESFET. These are dependent on device geometry and material parameters according to Liechti. He also described the noise behavior of the intrinsic MESFET. Liechti drew from his study that "for large drain voltages, the electrons reach their limiting velocity on the drain side of the channel (of the MESFET). In this region, the field has no influence on the carrier drift velocity." He then concluded, "this channel section cannot be treated as an ohmic conductor". Liechti's discussion was based on a maximum frequency of oscillation, f_u, at 46 GHz.

Liechti also studied the noise- and s-parameters of a GaAs MESFET at low temperatures and at a frequency of GHz (Ref 22:378). He used the same GaAs model as before. Through experimentation with a 1 micron gate length GaAs MESFET, he determined that it was capable of very low-noise performance at liquid-nitrogen temperatures. He also determined that the MESFET's transconductance increased with decreasing temperature, thereby raising the RF gain.

Pucel developed a small-signal equivalent circuit of the GaAs MESFET valid at frequencies up to X band (Ref 28) and used it in a mixer circuit. The mixer exhibited conversion gain at microwave frequencies based on the small-signal properties of the MESFET.

In Shur's work (Ref 18:612-618), a simple analytical model of the GaAs MESFET was proposed. Shur based his model "on the assumption that the current saturation in GaAs MESFETs is related to the stationary Gunn domain formation at the drain side of the gate rather than to a pinch-off of the conducting channel under the gate." Parameters calculated in the model were transconductance, gate-to-source, and drain-to-source capacitances, break-down voltage, saturation current, channel conductance, cut-off frequency, switching times, power-delay product, channel conductance, and charge under the gate. Two dimensional computer calculations were used to verify the results which agreed very closely with computer analysis results and 1 micron gate GaAs MESFET experimental data. Shur demonstrated that the gate length limitation was caused by stray gate-to-source and gate-to-drain capacitance. He determined that the gate length must be at least 1 micron for a GaAs MESFET.

Hower studied the theory, fabrication, and performance of an n-channel Schottky-barrier GaAs FET (Ref 19:199). He developed a lumped-element circuit model of the GaAs FET and used the model to determine its high performance. He used the model to derive common-source y-parameters using standard network analysis.

Dual-Gate Model. A study of the results of Furutsuka (Ref 20) will be presented in the dual gate characteristics section.

Selection of Models for Further Analysis

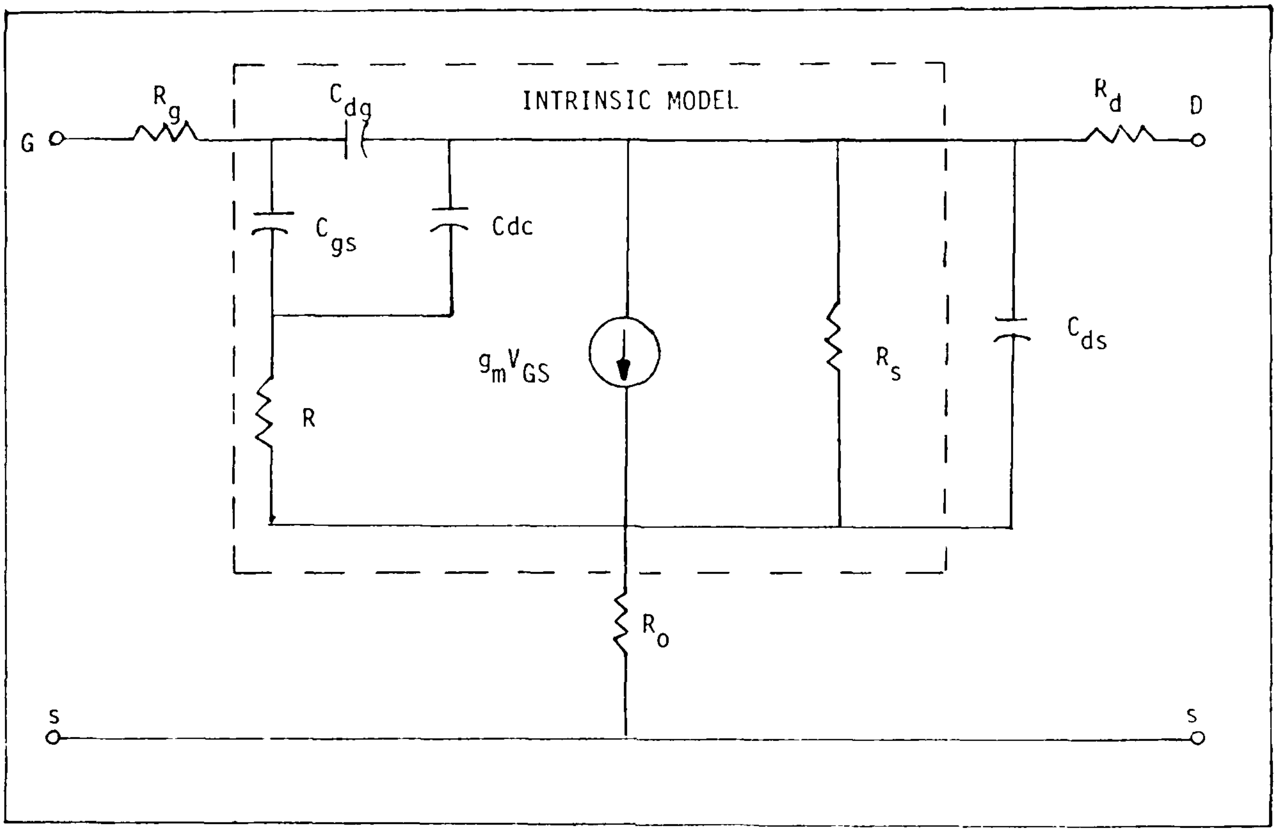
After preliminary analysis of the available models in the literature, the Liechti and Hower models were selected due to their ability to meet the criteria presented. These models are presented in Figures 10 and 11.

Both models are designed in a common-source configuration. These models are well suited to circuit design because they can be used to model the MESFET (with suitable biasing) as the active device of a switching circuit to provide an output which is 180° out of phase with the input. Additionally, a high input and output impedance exist (Ref 4:40). The Liechti model is adequate up to 12 GHz for 1 micron gate lengths (Ref 6:288). As for the Hower model, it is suitable for circuit design for frequencies up to 14 GHz for 3 micron gate lengths (Ref 19:192).

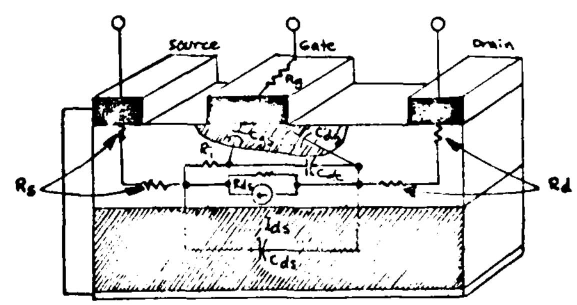
The Liechti and Hower models are both suitable for evaluation with the data from the Singer due to their potential to simulate the desired parameters on a family of I-V curves. For instance, R_o characterizes the MESFET in the ohmic region of the curves (Ref 15:164) at a value in the hundreds of ohms. Additionally, R_s models the MESFET in the saturation region at a value in the thousands of ohms. The drain current, I_D, is modeled by the constant current source shown in the figures.

The Liechti and Hower Models

Liechti's representation (Ref 6:285) of the equivalent circuit or model of a low-noise GaAs MESFET as shown in

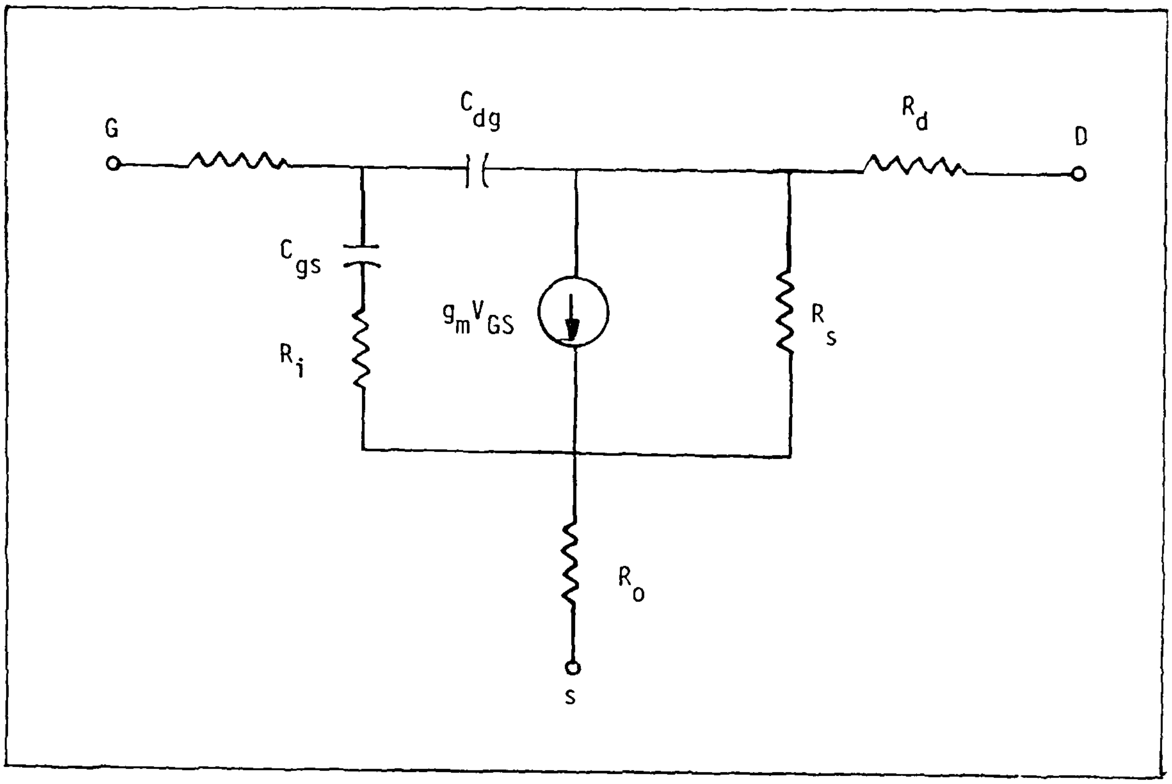


(a)

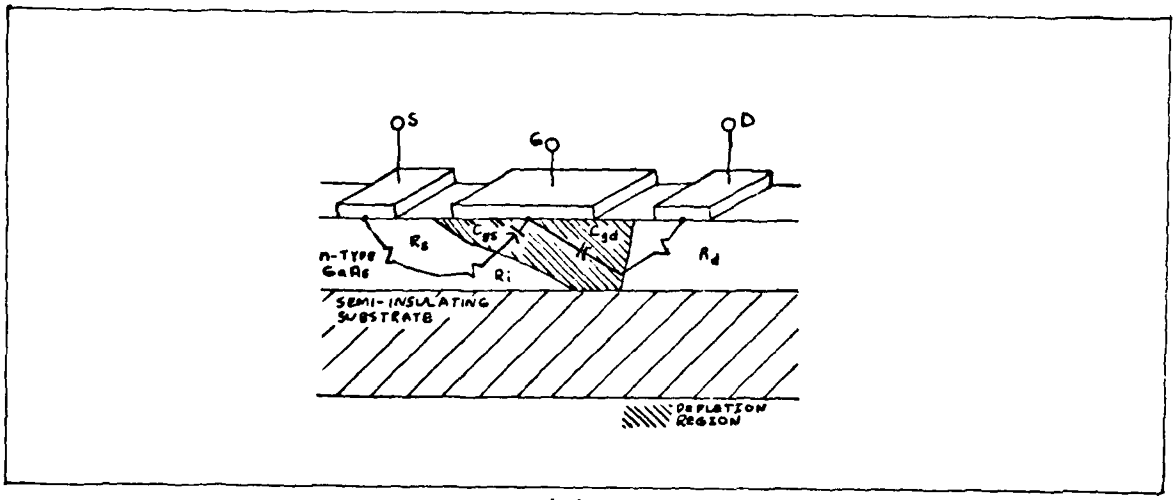


(b)

Figure 10. (a) Liechti's Equivalent Circuit Model of the GaAs MESFET. (b) Physical Origin of Circuit Elements (Ref 6:289).



(a)



(b)

Figure 11. (a) Hower's Equivalent Circuit Model of the GaAs MESFET. (b) Physical Origin of Circuit Elements (Ref 29:184).

Figure 10(a) is an RF equivalent of the MESFET. It simulates the n-channel as a distributed RC network. The common-source model is intended for operation in the saturated current region. The location of the elements of the model is shown in Figure 10(b) with the circuit parameters listed in Table II. The parameters are those obtained from an actual GaAs MESFET whose gate geometry was 1 micron (L_g) x 500 micron (W_g) with a donor concentration of $N_D = 1 \times 10^{17}$ cm^{-3}. The model takes into account the intrinsic as well as extrinsic elements of the MESFET (Ref 6:288).

Table II.

Equivalent-Circuit Parameters of a GaAs MESFET

with a 1 micron x 500 micron Gate

($N_D = 1 \times 10^{17}$ cm^{-3})

INTRINSIC ELEMENTS	EXTRINSIC ELEMENTS
g_m = 53 mmho	C_{ds} = 0.12pF
C_{gs} = 0.62pF	R_g -2.9 Ohm
C_{dg} = 0.014pF	R_d = 3.0 Ohm
C_{dc} = 0.02pF	R_s = 2.0 Ohm
R_1 = 2.6 Ohm	
R_s = 400 Ohm	

dc BIAS
V_{DS} = 5.0V
V_{GS} = 0.0V
I_D = 70.0mA

Hower's representation (Ref 19:184) of the model of a GaAs MESFET is shown in Figure 11. Hower's model is similar to Liechti's except for the absense of the parasitic elements R_g, C_{dc}, and C_{ds}.

The following devices (intrinsic and extrinsic) of the MESFETs are modeled in the Liechti and Hower models:

1. Gate-Metal Resistance
2. Gate-Source and Gate-Drain Capacitances
3. Dipole Layer Capacitance
4. Source and Drain Resistances
5. Drain - Source Capacitance
6. Drain - Source Resistance
7. Current Source

The modeled devices will be described in the following subsections.

Gate-Metal Resistance. The gate resistance (extrinsic) Figure 10(a) is modeled by

$$R_g = \rho\ Z_g/12t_gL_g \tag{4}$$

where ρ(2.75x10^{-6} ohm-cm), t_g ($\triangleq$0.5 micron), L_g (1 micron) and Z_g (100 micron) are the specific resistivity, approximate thickness, length, and width of the gate respectively for MESFETs fabricated by AFWAL/AA (Ref 20:581). Substituting these values into the above equation yields $R_g \approx 1.80$ ohms.

Gate-Source and Drain-Gate Capacitances. The gate-source capacitance, modeled by C_{gs} (Figure 10) and drain-gate capacitance (Figure 10 and 11) by C_{dg}, are both intrinsic elements of the MESFET according to Liechti. C_{gs} and C_{dg} represent the total gate-to-channel capacitance, $C_{dg} + C_{gs}$ (Ref 6:288). According to Hower, C_{dg} is a feedback capacitance that accounts for the effect of field lines that emanate from charges near the drain contact and terminate on the gate. From Liechti (Ref 6:289), R_g and C_{dg} form a time constant,

$$\tau_{RC_1} = 1/f_{RC_1} = 2\pi R_g C_{dg} \qquad (5)$$

C_{gs} charges through a channel resistance, R_i, and together they form a time constant given by

$$\tau_{RC_2} = 1/f_{RC_2} = 2\pi R_i C_{gs} \qquad (6)$$

(Ref (19:184)

Expressions for C_{dg} and C_{gs} have been derived taking into account Z_g, L_g, V_i, V_g, V_{Bi}, and A_o (Ref 18:615). These expressions can be simplified when $V_i << V_{BI} - V_g$. Then,

$$C_{dg} = C_{gs} = 1/2\sqrt{2}\ Z_g L_g((\varepsilon_o \varepsilon q N_D)/(V_{Bi}-V_G))^{1/2} = 1/2\varepsilon_o \varepsilon Z_g L_g/A_o$$

(Ref 18:615) (7)

Dipole Layer Capacitance. The dipole layer capacitance modeled by C_{dc} (Figure 10), is an intrinsic element according to Liechti (Ref 6:288). C_{dc} models the capacitance of the distribution of space charge beneath the deplection region.

Source and Drain Resistances. The source and drain resistances modeled by R_o, and R_d (Figures 10 and 11) respectively, are both extrinsic or parasitic elements (Ref 6:288). According to Hower (Ref 19:183-184), R_o and R_d are as shown in Figure 11.

R_o is used to model the MESFET channel in the linear region of an I-V curve.

<u>Drain-Source Resistance.</u> The drain-source resistance is modeled by R_s (Figures 10 and 11). R_s characterizes the channel in the saturated current region (Ref 15:163).

<u>Current Source.</u> The drain current is modeled by the current source, I_D (Figures 10 and 11). According to the models by Liechti and Hower, the current source is dependent upon the voltage, v_c, developed across C_{gs} (Ref 6:288). The trans-admittance, g_m, is related to I_D by

$$I_D = y_m v_c \tag{8}$$

and

$$y_m = g_m e^{-j\omega\tau_o} \tag{9}$$

where τ_o is the phase delay "reflecting the carrier transit time in the channel section where $E>E_p$:(Ref 6:288).

Up to 12GHz, y_m is characterized by a frequency-independent magnitude, the transconductance g_m, and τ_o. At DC, $\omega = 0$, and therefore $y_m = g_m$ and $I_D = g_m V_c$. At low frequencies, according to Millman (Ref 11:320), I_D is proportional to the gate-to-source voltage, V_{GS}. Therefore, for a DC model of the GaAs MESFET, it is assumed that

$$I_D = g_m V_{GS} \tag{10}$$

<u>Modification and Analysis</u>

In this section, the models developed by Liechti and Hower will be modified in order to omit those elements that will not be significant in determining the DC parameters of the MESFET. Kirchoff's voltage law will then be applied to the resulting proposed model to determine a useful relationship between I_D, V_{GS}, and V_{DS} of the MESFET in the saturated current region. I-V curves taken from an actual single-gate MESFET at AFWAL/AADE will then be used in correlating these DC parameters to those obtained by the equation relating V_{GS} and V_{DS} to I_D.

The capacitances, C_{dg}, C_{gs}, C_{dc}, and C_{ds}, all represent extremely high complex impedances at DC and can be neglected (Ref 15:168). According to Millman (Ref 11:321), no feedback exists at low frequencies from output to input in the FET, and it will be assumed that this is true for the MESFET. With this being the case, the capacitances can be removed from the model. As a result, no current (at DC) flows from the gate to the drain or source via R_g and R_i. Therefore, these resistances can be removed. Current flows, of course, through the drain via the low valued resistance, R_d (3 ohms) (Ref 6:288). R_s and R_o are significant as pointed out in the following analysis and will not be removed. The modified model is shown in Figure 12.

The actual characteristic I-V curves shown in Figure 13 (obtained through measurement as described in Appendix A) will be applied to the modified model as shown in Figure 12. Referring to Figure (characteristic curves of a source follower, Figure 1(A)), I_{DSS} is determined to be about 11.6 mA at V_{GS} = 0. The transconductance, g_m, is found from the curves using equation (13). According to (13), g_m is the ratio of a change in drain current due to a change in gate

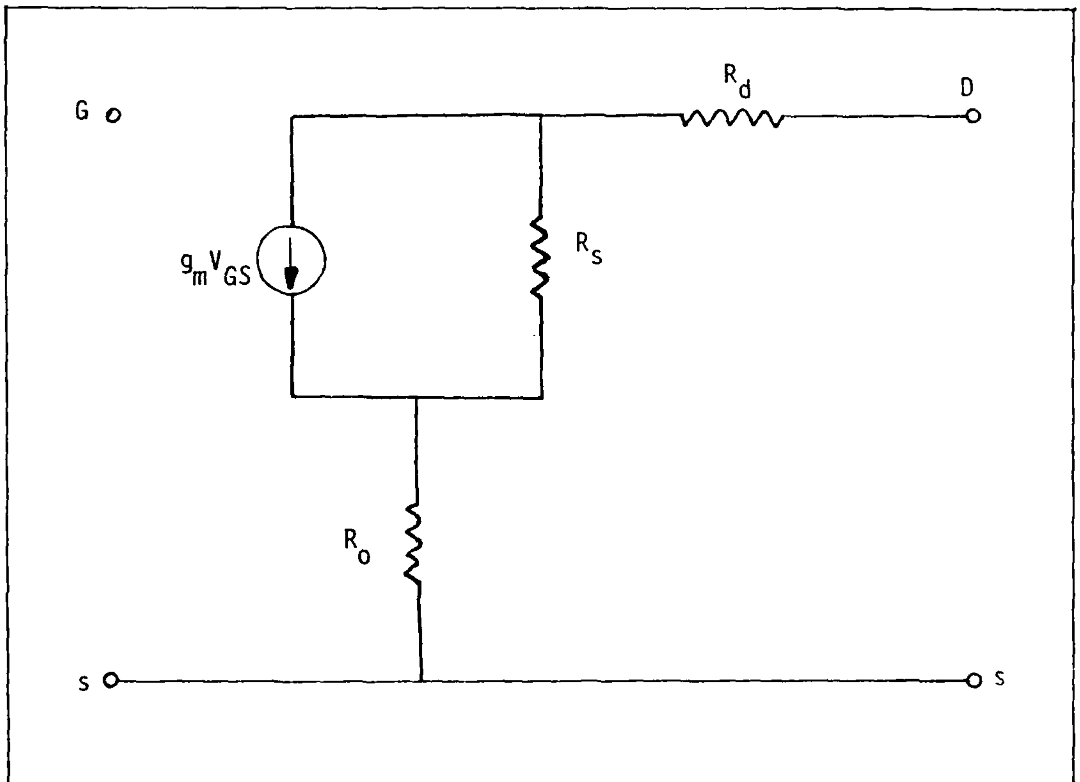


Figure 12. Modified DC Equivalent Circuit Model of the GaAs MESFET.

voltage at an applied V_{DS}. Selecting V_{DS} at 5.0V places the MESFET in the saturation region.

$$g_m = \Delta I_D/\Delta V_{GS} = (I_{D2}-I_{D1})/V_{GS_2}-V_{GS_1})\Big|_{V_{DS}=4.0V} \quad (13)$$

From Figure 13, at V_{DS} = 4.0V, I_{D_2} = 12.2 mA at V_{GS_2} = 0.0V and I_{D_1} = 10.0 mA at V_{GS_1} = -1.0V. Applying these parameters to 13, g_m = 2.2 millimho (mmho) (Ref 12:86).

Operation in the linear region can be determined using the inverse of the slope (Ref 15:163 and Ref 11:316).

$$R_o = \Delta V_{Ds}/\Delta I_D = (V_{DS_2}-V_{DS_1})/(I_{D_2}-I_{D_1})\Big|_{V_{GS}} \quad (14)$$

Values of R_o as well as other DC parameters for g_m, I_D, V_D, V_{GS}, V_{DS},I_{DSS} and R_d are listed in Table XVII, Appendix K, R_o depicts the ohmic linear region of the MESFET prior to saturation for a given applied V_{GS}. Using this equation, I_D can be solved for different values of applied V_{DS} (at a V_{GS}) in the linear region as I_D approaches saturation.

At saturation, I_D remains constant while V_{DS} is varied. The slope of the saturated region (at a given V_{GS}) is the inverse of the output resistance, R_s (Ref 11:162), where

$$R_s = (V_{DS_2}-V_{DS_1})/(I_{D_2}-I_{D_1})\Big|_{V_{GS}} \quad (15)$$

R_s is usually larger than R_o. Values of R_s for each V_{GS} from Figure 13 are listed in Table XVII, Appendix K.

The pinchoff voltage, V_p, according to Figure 13, is about -8.0V. This value is quite large compared to Liechti's value of V_p at -2.5V.

Operation in the saturated current region can be depicted by expressing I_D as a function of V_{DS} and V_{GS} using the measured data from Figure 13. A simple approach to modeling the measured data would be to begin by applying Kirchoff's voltage law to the modified model of Figure 12. Applying a voltage V_{DS} and using conventional current directions, I_D can be calculated from the following analysis:

$$V_{DS} = R_d I_D + R_s(I_D - g_m V_{GS}) + R_o I_D \qquad (16)$$

$$V_{DS} = (R_d + R_s + R_o)I_D - R_s(g_m V_{GS}) \qquad (17)$$

Therefore,

$$I_D = (V_{DS} + R_s g_m V_{GS})/(R_d + R_s + R_o) \qquad (18)$$

Equation (18) is intended for use in the saturated current region. I_D here is represented by the characteristic equation

$$I_D = I_{DSS}(1 - V_{GS}/V_p)^2 \qquad (19)$$

According to $(I_D = g_m V_{GS})$,

$$g_m V_{GS} = I_{DSS}(1 - V_{GS}/V_p)^2. \qquad (20)$$

Substituting (20) into (18),

$$I_D = (V_{DS} + I_{DSS} R_s (1 - V_{GS}/V_p)^2)/(R_d + R_s + R_o) \qquad (21)$$

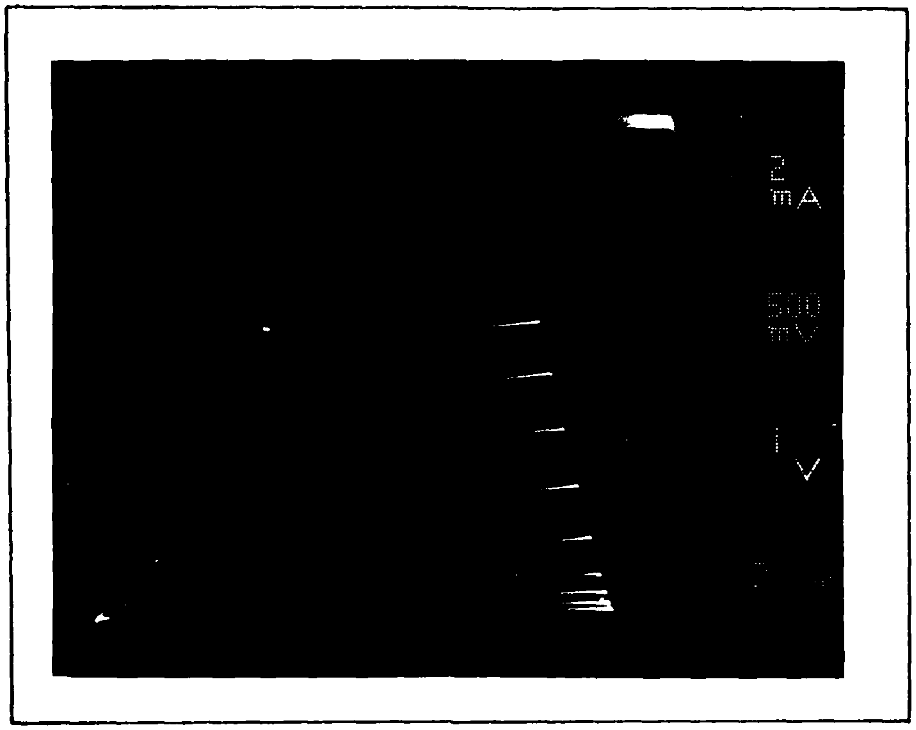


Figure 13. Manually Tested SOURCE FOLLOWER Characteristics.

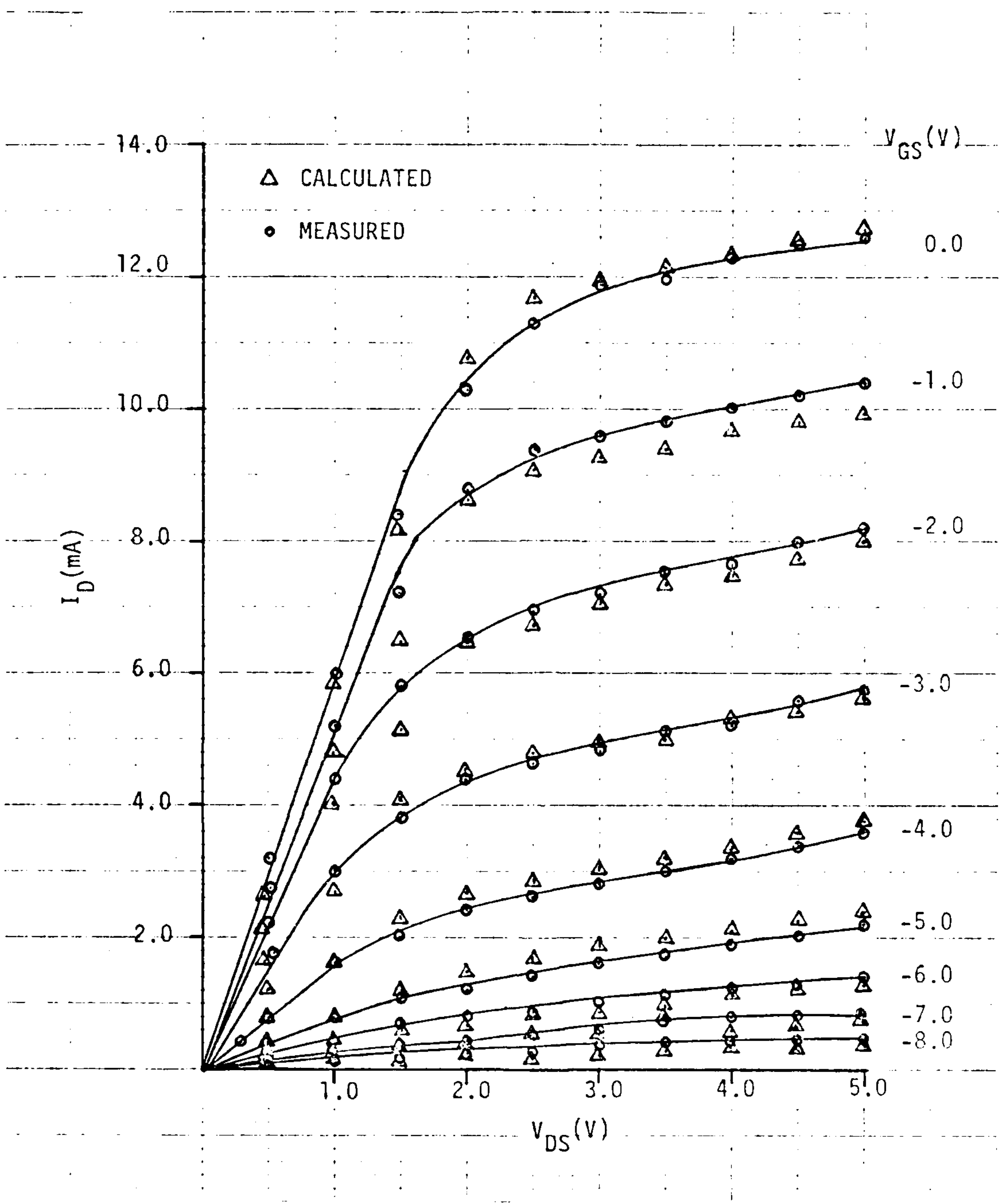


Figure 14. Derived I-V Characteristics Using the Proposed MESFET DC Model.

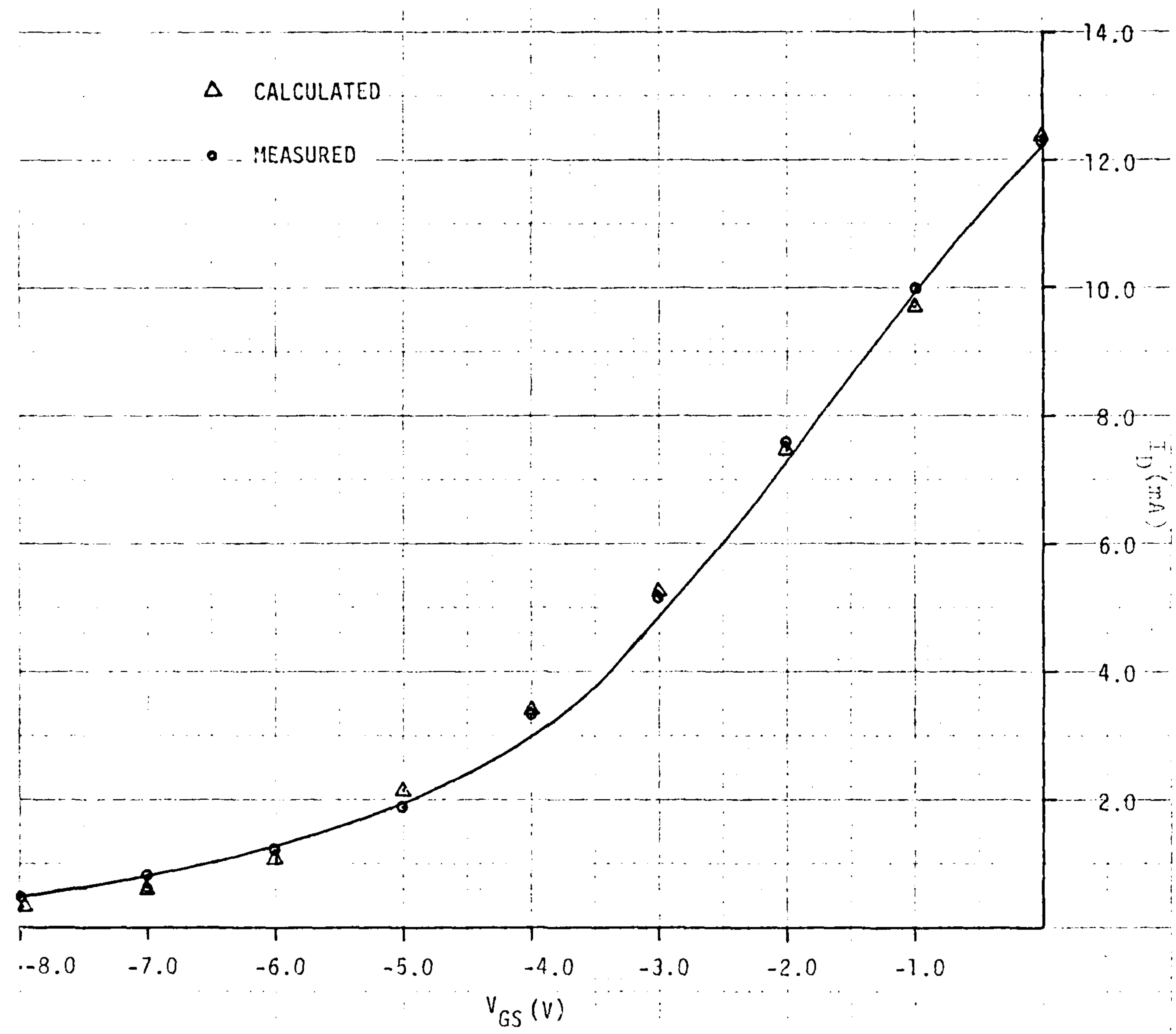


Figure 15. Transfer Characteristic of the Proposed MESFET DC Model.

Equation (21) is a function of V_{DS} and V_{GS} and is applicable only in the saturated current region of Figure 13. Curves obtained for I_D vs. V_{DS} with V_{GS} as a parameter using the parameters from Table XVII as applied to (21) are also shown in Figure 14. The linear region of the curves (at a given V_{GS}) is determined from

$$R_o = \Delta V_{DS}/\Delta I_D \tag{22}$$

It can be seen in Figures 14 and 15 that the calculated model data in comparison to the measured data differ by as much as 0.4mA in the saturated current region. Further observation of the figures as well as reference to Table XVII, Appendix K, indicate an approximate correlation of the model to the actual measured characteristics of Figure 12.

Dual Gate Characteristics

By referring to Figure 2(a), it can be seen that the NAND/NOR circuit under study includes both single and dual gate MESFETs. The dual gate MESFET is identical to the single gate MESFET except that it has two gate electrodes between the source and drain contacts with both gates modulating the drain current. The dual gate is capable of switching 15-25% less current at V_{GS} = 0.0v than the single gate when the gate potentials are maintained at levels typical for logic circuit operation (Ref 4:6). The advantages of the dual gate over the single gate MESFET are (1) increased functional capability due to the presence of two independent control gates, such as gain control and signal mixing, and (2) reduced feedback resulting in an improvement in power gain and stability (Ref 20:580).

The Dual Gate Model. The dual gate device can be visualized as two separate single gate MESFETs connected in cascade as shown in Figure 16 (Ref 8:462). The output current of $MESFET_1$, flows directly into the channel of $MESFET_2$. If the potential between the two gates, V_{DS_1}, is greater than the threshold voltage for current saturation, $V_{DS_{(SAT)}}$, then $MESFET_1$ acts as an ideal current source. The gate bias, V_{GS_2}, applied at the second gate, controls the drain voltage V_{DS_1} of the first transistor. To allow $MESFET_2$ to carry the DC current from $MESFET_1$, V_{DS_1} adjusts to establish the proper gate-to-source bias $V_{GS_2}-V_{DS_1}$. No DC current flows into the second gate as long as V_{GS_2} (positive) remains about 0.5v below the drain voltage and the first gate bias is less than or equal to zero ($V_{GS_1} \leq 0$).

In a paper by Furutsuka (Ref 20:580), the operation and characteristics of the dual gate MESFET were treated by combining the analyzed characteristics of two single gate MESFETs operated under the same drain current. His study also included high-frequency noise behavior analyzed on the basis of Statz's model (Ref 29:559). Statz's model is an equivalent circuit model for the MESFET and includes the noisy parasitic elements inherent in the MESFET. Statz's model is basically similar to Liechti's (Ref 6:289) except with the addition of noise generators. Using Statz's model, Furutsuka

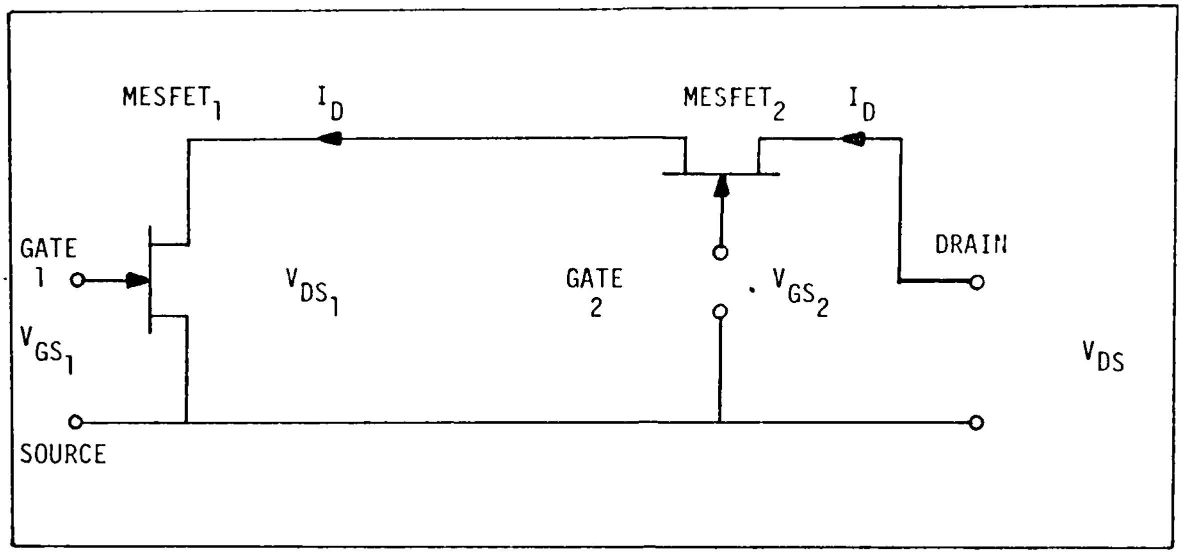


Figure 16. Dual-Gate MESFET Modeled as Two Single-Gate MESFET's Connected in Cascade (Ref 8:461).

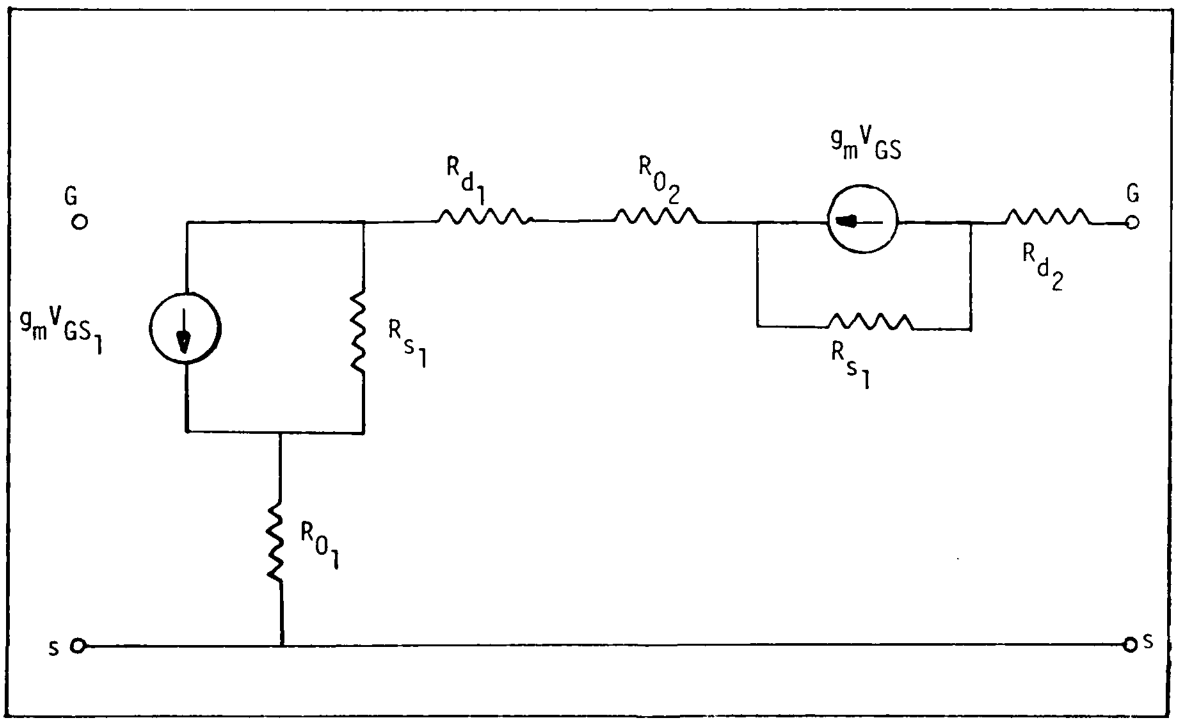


Figure 17. Modified Dual-Gate MESFET Model (Ref 8:462).

calculated the drain current I_D and the channel lengths of the carrier velocity unsaturated and saturated regions of both MESFETs of the dual gate as a function of the gate bias V_{GS_1} and V_{GS_2}. They were also calculated as a function of the gate bias V_{GS_1} and V_{GS_2}, and V_{DS}. These characteristics were obtained by adjusting I_D to be the same through $MESFET_1$ and $MESFET_2$ with the voltage drops across the two MESFETs and the source and drain resistances summed to equal V_{DS}.

An equivalent circuit of the dual gate MESFET, [illegible] by Furutsuka (Ref 20:581), is a combination of two single gate MESFET models developed by Statz (Ref 29:559) complete with parasitic elements and noise generators. Since the DC parameters of the dual gate MESFET are of primary importance in this study, the parasitic elements and noise generators. Since the DC parameters of the dual gate MESFET are of primary importance in this study, the parasitic elements and noise generators are shown removed, for the parasitic elements of the single gate MESFET, in Figure 17.

Summary

In this chapter, single and dual gate models were proposed and studied. A search of the available literature was conducted to study the single and dual gate models. The single gate model was correlated with actual measured characteristics. Procedures developed to test the devices of Figure 1(a) will be presented in Chapter IV.

IV. AUTOMATED DC PARAMETER TESTING PROCEDURE DEVELOPMENT

In the automated testing of the devices in Figures 1 and 2, several fundamental considerations had to be established before developing the automated test program. Additionally, it was necessary to understand the test language and how it could be used to test devices that had never before been tested on this system. It was also required that an ability to validate the test results be available.

The purpose of this chapter is to present the conditions and requirements established prior to testing and the approach and techniques (basic testing and programming) used in the attempt to validate results obtained through automated testing. Experimental results will be presented and compared to actual results in an attempt to validate the developed programs. Problems experienced in the testing will be presented as well as the attempted approach to resolving them.

Test Considerations

Before attempting to automatically test the circuit in Figure 1, facility with the Singer tester's Elucidate software was required. A 4-bit accumulator fabricated at AFWAL/AADE was tested on the Singer as an exercise in obtaining an overall understanding of the Elucidate software as well as the system's hardware. Conclusions drawn from this exercise are presented in Appendix J. The conclusions obtained from this testing effort were used to determine the capabilities and limitations of the system. In addition, an understanding of the methods used to test the devices in Figures 1 and 2 manually was required before any automated testing was conducted. This is documented in Appendix A. Conclusions drawn from this section were used to develop programs to automate the manual process.

In order to automatically test devices at the wafer level, it was necessary to develop a means to interface the Singer with the devices on the wafer. A special probe card was developed to provide the necessary interface capability. Further discussion on the probe card is found in Appendix G.

Test and Programming Techniques

The DC parameters for the various devices within the GaAs gate circuit which required testing are shown in Tables III and IV. These basic parameters are characteristic of any equivalent FET, diode or resistor in discrete form.

An organizational flowchart of the proposed program to test the devices is shown in Figure 18. A top-down approach was stressed in order to reduce overall complexity and redundancy. The design of the overall program was to emphasize a well organized approach to test the devices. Accordingly, the program was organized in device by device sections. The DC parameters of each of the devices on a chip were to be tested separately before the next chip was placed under the probe card for continued automated testing. The details of the Singer system which influence the execution of this scheme are discussed in Appendix B. In addition, further details and procedures to automate the chip by chip testing of the NAND/NOR circuit are included in Appendix H.

Table III

Basic DC Parameters to be Tested For Each MESFET In Figure 1.

	MESFET DEVICES				
DC PARAMETERS	SOURCE FOLLOWER(SF)	CURRENT SOURCE(CS)	ACTIVE LOAD(AL)	SINGLE GATE(SG)	DUAL GATE(DG)
VDS at VGS = 0 (Volts)	*	*	*	*	*
IDSS(mA)	*	*	*	*	*
LINEAR ON-RESISTANCE(RO)(Ohms)	*	*	*	*	*
SATURATION RESISTANCE(RS)(Ohms)	*	*	*	*	*
PINCH-OFF VOLTAGE(VP)(Volts)	*	*		*	*
TRANSCONDUCTANCE(GM)(Millimhos)	*	*		*	*
BREAKDOWN VOLTAGE(VB)(Volts)	*	*	*	*	*

Table IV

Basic DC Parameters to be Tested for Schottky Diodes and Resistors in Figure 1.

	DEVICE		
DC PARAMETERS	SCHOTTKY DIODES	TEST RESISTOR	PROBE RESISTOR
FORWARD THRESHOLD VOLTAGE(VF) (Volts)	*		
REVERSE THRESHOLD VOLTAGE(VR) (Volts)	*		
OHMIC RESISTANCE(OHMS)		*	*

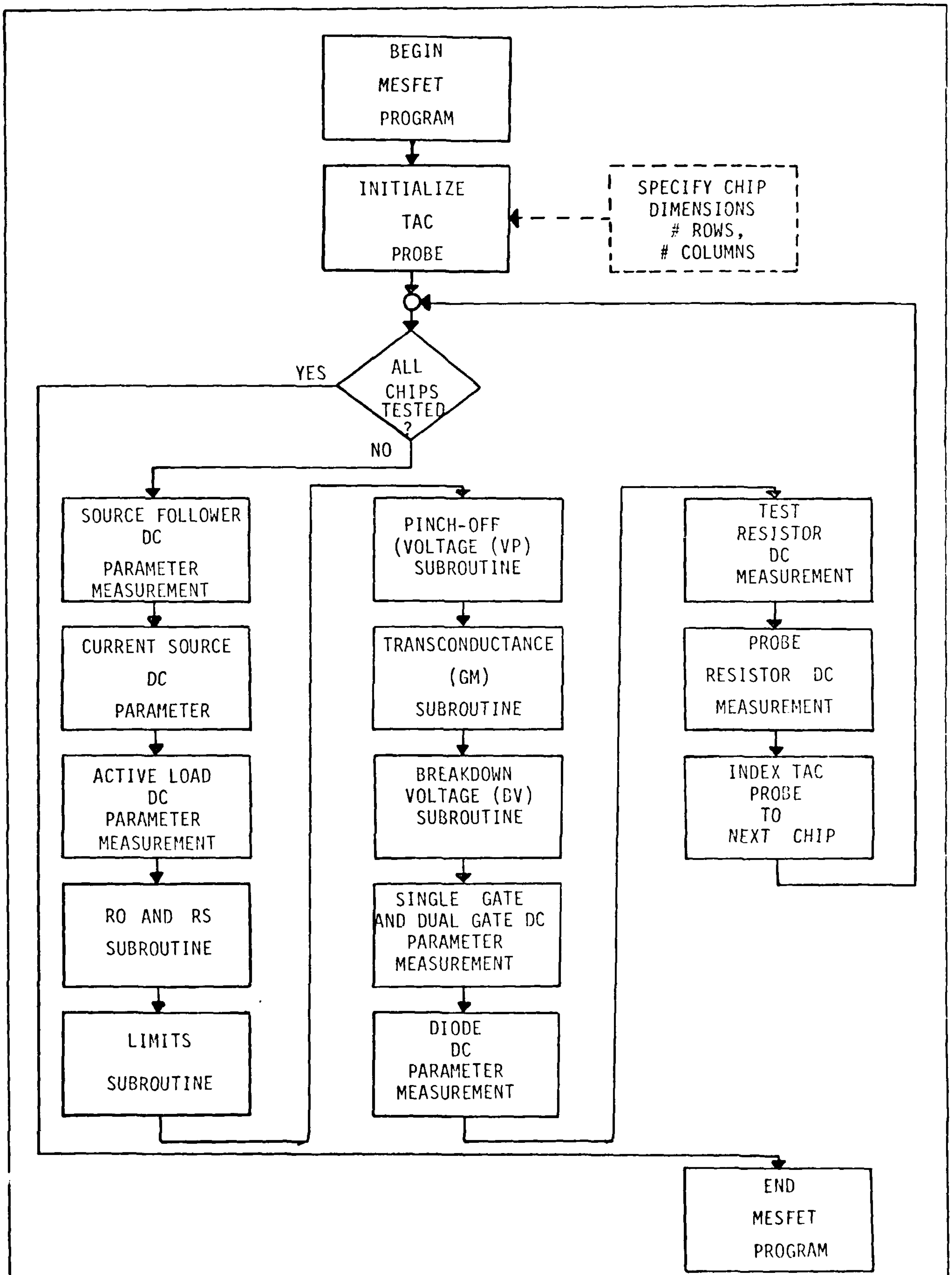


Figure 18. MESFET Program Organizational Flowchart.

Computational and comparison subroutines, RO, RS, LIMITS, VP, GM, and BV were included as such since they are common to all of the devices to be tested. Routines IDSS and VDS (not shown in Figures 18) were included in each device section. They require simple measurements and do not require as many lines of code as did the other DC parameters. To avoid confusion, physical parameters will henceforth be referred to by their variable names in the test software, e.g., IDSS instead of I_{DSS}.

System Preparation

Prior to implementing the DC parameter measurement program, MESFET, matrix pin numbers and power supplies had to be determined. A map of the pin numbers for each device in Figures 1 and 2 was determined during construction of the probe card. The probe card was used to interface the matrix system of the Singer tester with the devices at the wafer level. The pin assignments for each device are shown in Table XII, Appendix G, with Figure 1 drawn again with pin number assignments in Figure 19. The available power supplies to choose from are described in Appendix B. VS1, VS2, and VS5 were chosen due to their characteristics and availability. The VS1 and VS2 power supplies were chosen to apply VGS voltages. VS5 was chosen for its capability to measure currents after it was connected to a device. VS5 was set to a particular VDS and was then capable of measuring currents when the READ VS5 command was executed. A further discussion of the Elucidate software is found in Appendix C.

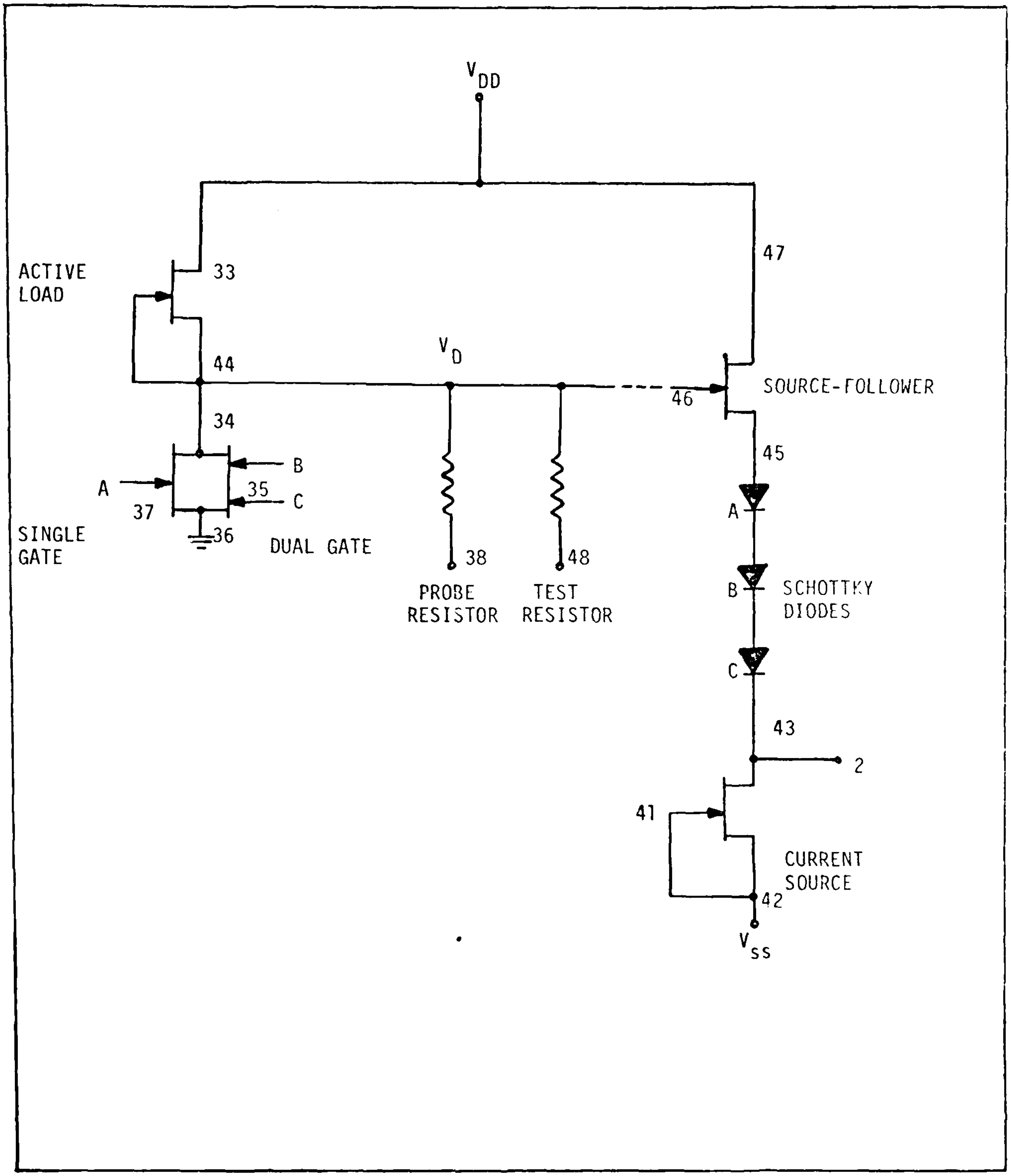


Figure 19. NAND/NOR Circuit Schematic with Matrix Pin Assignments.

MESFET Program Layout

In the following sections, the device sections and subroutines are explained in the following sequence:

1. Parameters to be tested.
2. Calculations and comparisons involved (subroutines only).
3. Algorithm (Device and VP only).
4. Flowchart.

The order of presentation will be similar to the order in the organizational flowchart, Figure 18.

Source Follower (SF) DC Parameter Measurement. According to Table III, the DC parameters to be tested for the Source Follower (SF) were VDS, IDSS, RO, RS, VP, GM, and BV. In order to measure IDSS, VP, and BV, it was necessary to initialize VDS so that the device was operating in the saturation region. From observation of the SF I-V curves in Figure 51, Appendix A, obtained through manual testing, VDS was set at 5.0V. This initial voltage setting was used throughout the automated testing program for measuring IDSS, and later VP.

An algorithm used to describe the testing of SF will now be described:

1. Condition Singer test system (See Appendix B) for testing using VS5=VDS, VGS=0, and the following pin connections.

PIN 47 = DRAIN

PIN 46 = GATE

PIN 45 = SOURCE

At VGS = 0, the gate is shorted to GND.

2. CONNECT the voltmeter between drain and source.

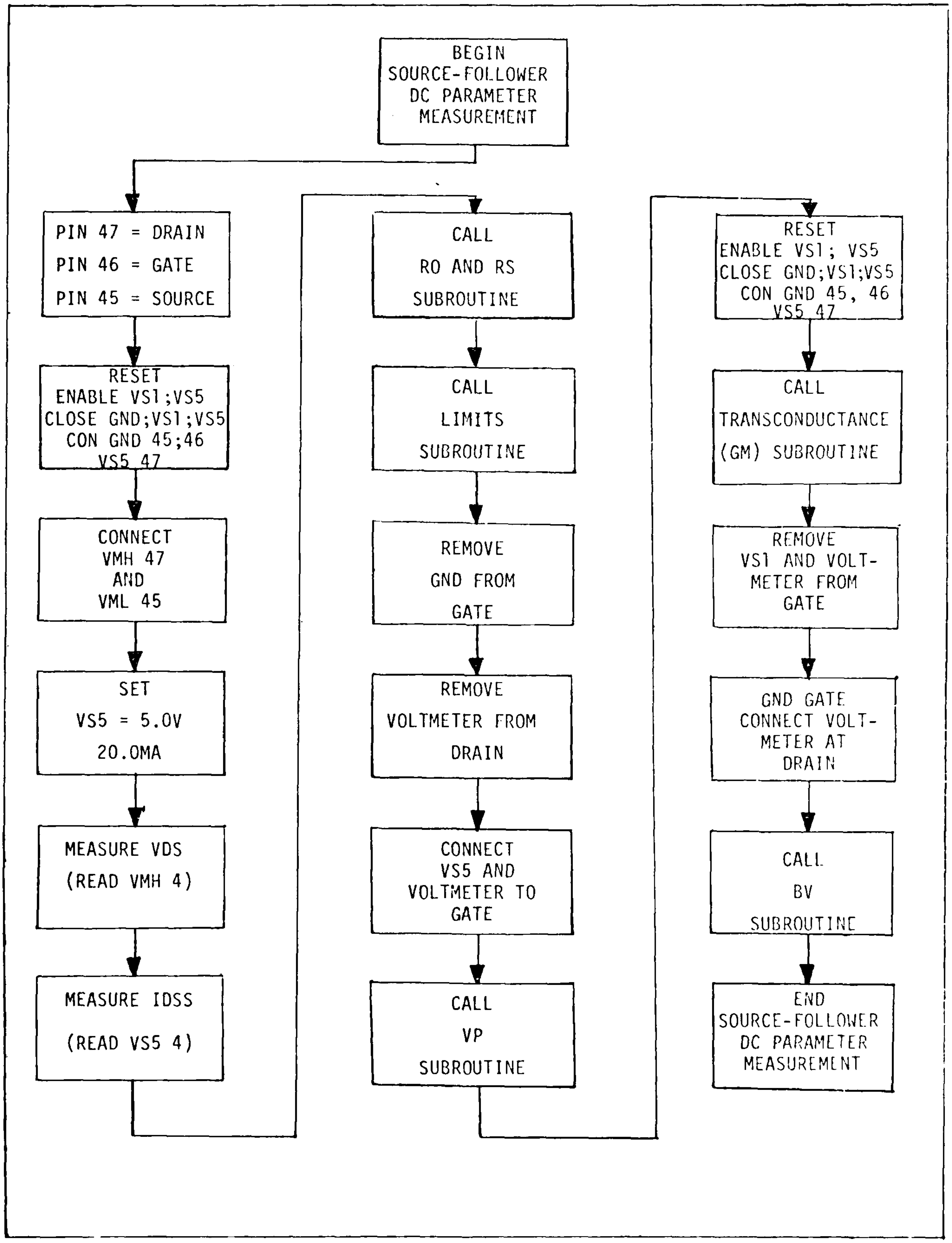


Figure 20. SOURCE FOLLOWER (SF) DC Parameter Measurement Flowchart.

3. SET VS5 at 5.0V at a clamp of 20.0mA.
4. READ the voltmeter and RPINT reading: VDS at 5.0V.
5. READ VS5: IDSS at VDS = 5.0V.
6. Equate IDSS to variables for use later in the LIMITS subroutine.
7. PRINT IDSS.
8. Call RO and RS subroutine.
9. Call LIMITS subroutine.
10. Remove GND from gate (Pin 46) and the voltmeter from the drain (Pin 47).
11. CONNECT VS1 and the voltmeter to the gate.
12. Call PINCH-OFF VOLTAGE (VP) subroutine.
13. RESET and condition system.
14. Call TRANSCONDUCTANCE (GM) Subroutine.
15. Remove VS1 and voltmeter from gate.
16. GND gate and CONNECT voltemter at drain to measure BREAKDOWN VOLTAGE (BV) subroutine.
17. Call BV subroutine.
18. End SF DC parameter measurement.

A flowchart for the Source Follower DC parameter measurement is shown in Figure 20.

<u>CURRENT SOURCE (CS) DC Parameter Measurements.</u> The DC parameters, algorithm and flowchart (Figure 21) for the Current Source DC parameter measurement are the same as for the Source Follower except for the different pin connections.

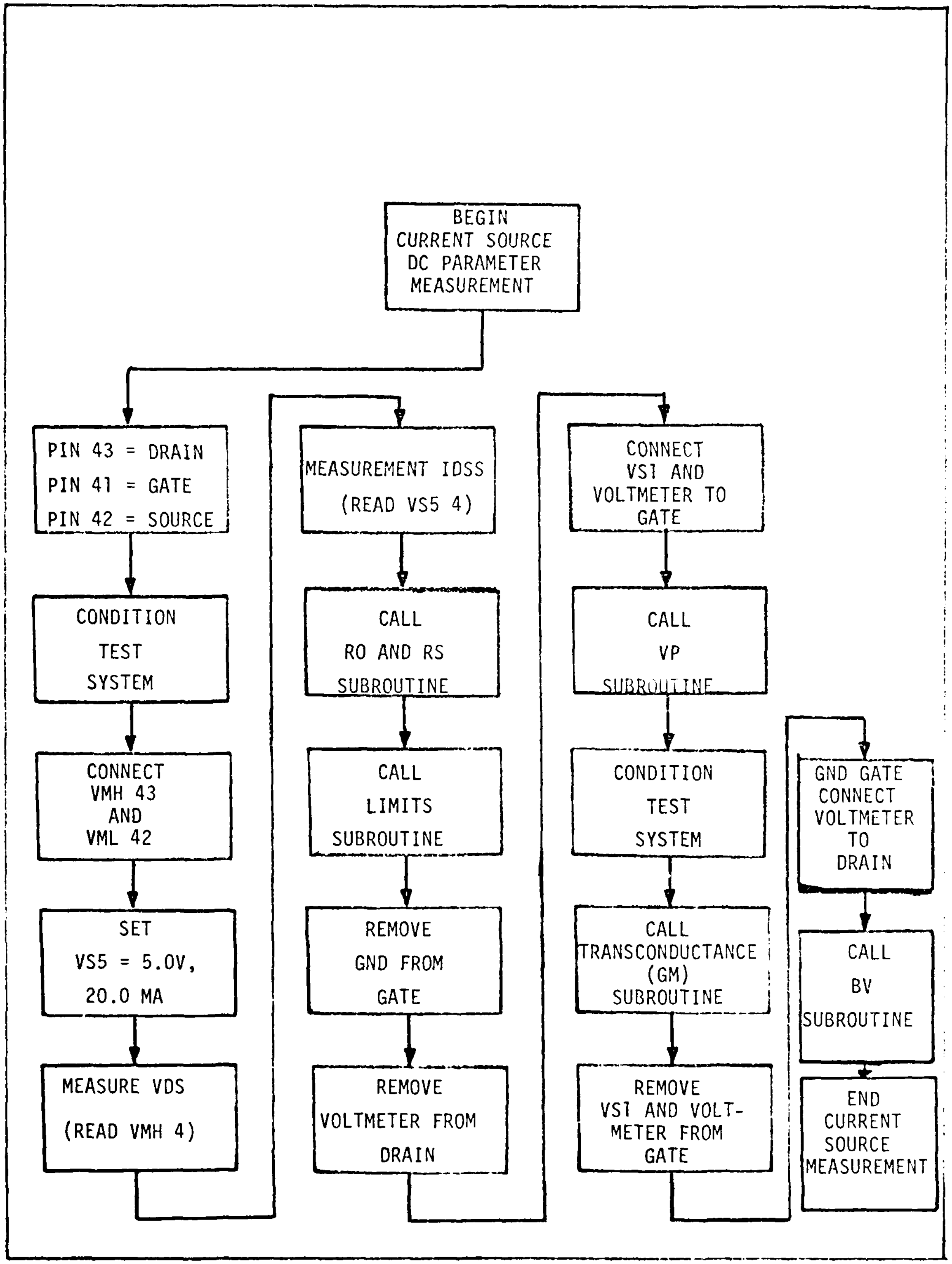


Figure 21. CURRENT SOURCE (CS) DC Parameter Measurement Flowchart.

The pin connections for the current source are the following:

PIN 43 = DRAIN

PIN 41 = GATE

PIN 42 = SOURCE

To condition the test system for testing the CURRENT SOURCE, the following commands must be used:

RESET

ENABLE VS1;VS5

CLOSE GND; VS1;VS5

CON GND 42;41;VS5 43

ACTIVE LOAD (AL)

DC Parameter Measurement. As shown in Table III, the DC parameters to be tested for the ACTIVE LOAD were VDS, IDSS, RO,RS, and BV. VDS was initialized at 5.0V so that the device was operating in the saturation region in order to measure IDSS. The gate and source of the Active Load are physically connected within the circuit.

An algorithm used to describe the testing of the ACTIVE LOAD will now be described.

1. Condition Singer system for testing using the following pin connections:

PIN 33 = DRAIN

PIN 44 = SOURCE

RESET

ENABLE VS5

CLOSE GND; VS5

CON GND 44; VS5 33

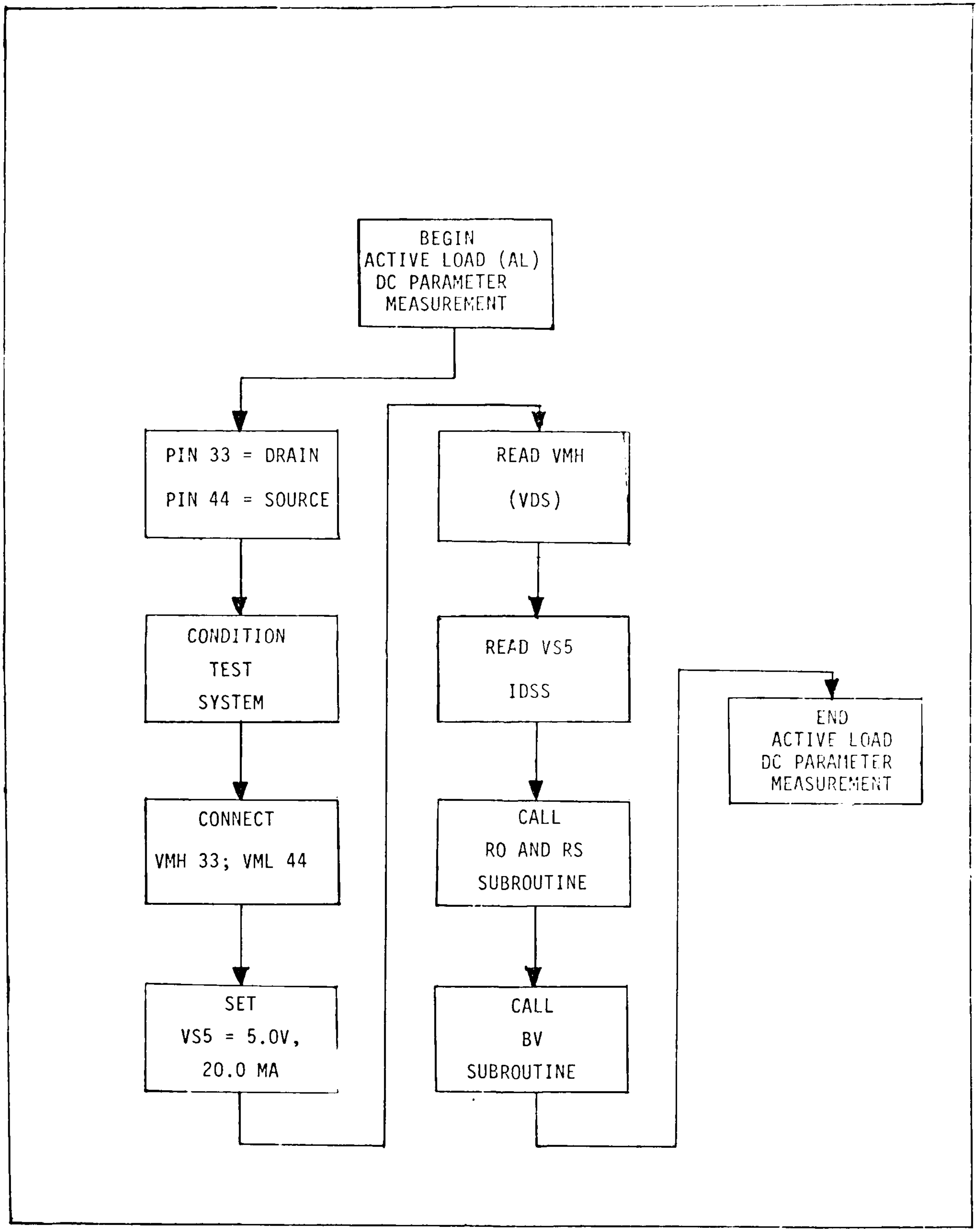


Figure 22. ACTIVE LOAD (AL) DC Parameter Measurement Flowchart.

2. CONNECT the voltmeter between drain and source.

3. SET VS5 at 5.0V at a clamp of 20.0MA.

4. READ the voltmeter and print reading: VDS at 5.0V

5. READ VS5 and print reading: IDSS

6. Call RO and RS subroutine

7. Call BV subroutine

8. End Active Load DC parameter measurement

The flowchart for the Active Load DC parameter measurement is shown in Figure 22.

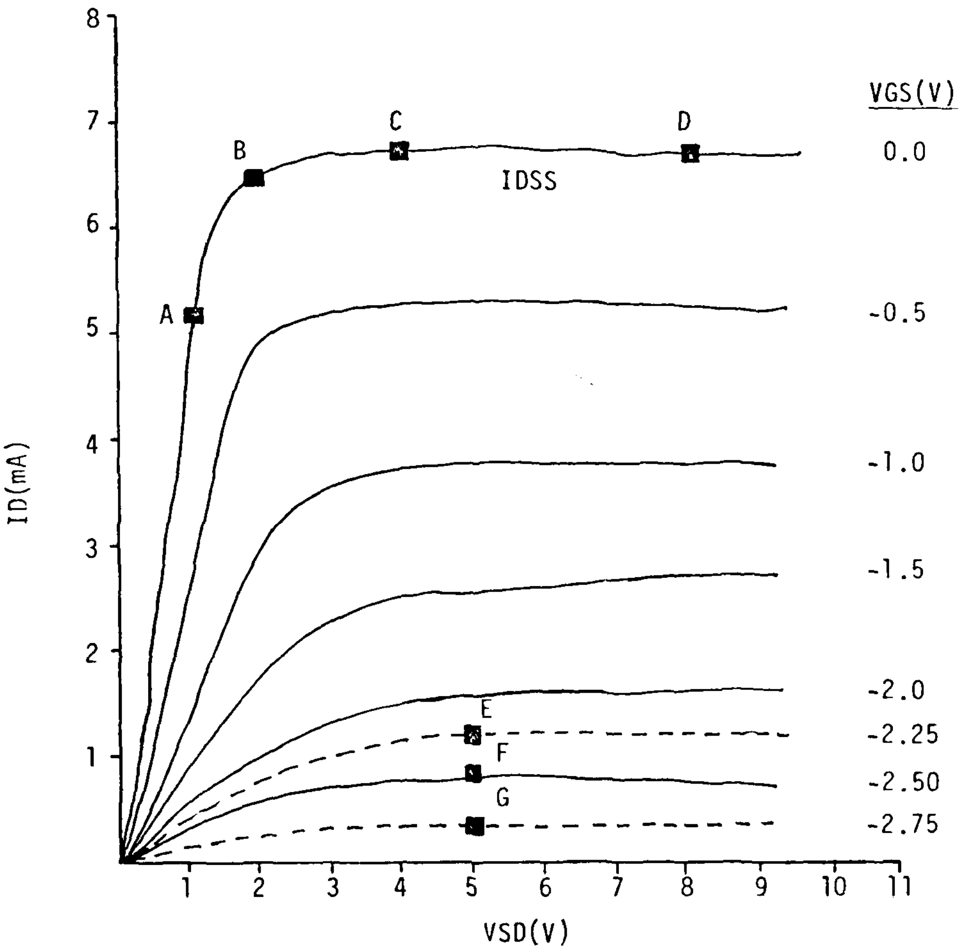
LINEAR ON-RESISTANCE (RO) and SATURATION RESISTANCE (RS) Measurement Subroutine. The parameter to be tested in this subroutine are the linear on-resistance (RO) and the saturation resistance (RS) of the MESFET channel at VGS = 0. The calculation involved in the subroutine are:

$$RO = \frac{VDS2-VDS1}{ID2-ID1},\ VDS2=2.0V, VDS1 = 1.0V \qquad (23)$$

$$RS = \frac{VDS2-VDS1}{ID2-ID1},\ VDS2=7.0V,\ VDS1=4.0V \qquad (24)$$

where ID1, 2 are drain currents measured at VDS1,2.

The voltage settings used in measuring RO place the MESFET in the linear region of the I-V curve, whereas the settings used in measuring RS place the MESFET in the saturation region. Figure 23 graphically depicts the points to be measured. No comparisons are made in this subroutine-only straightforward calculations are involved. The flowchart for the RO and RS subroutine is shown in Figure 24. Prior to entering the subroutine, the gate must be shorted to the source, VS5 connected to the drain, and the source grounded.



A=(VSD1(RO)=1.0V,ID1(RO))
B=(VDS2(RO)=2.0V,ID2(RO))
C=(VDS1(RS)=4.0V,ID1(RS))
D=(VDS2(RS)=7.0V,ID2(RS))

E=ID=1.5% of IDSS
F=ID=1.0% of IDSS
G=ID=0.5% of IDSS

Figure 23. Graphical Method Implemented on the Singer to Determine RO, RS, and VP.

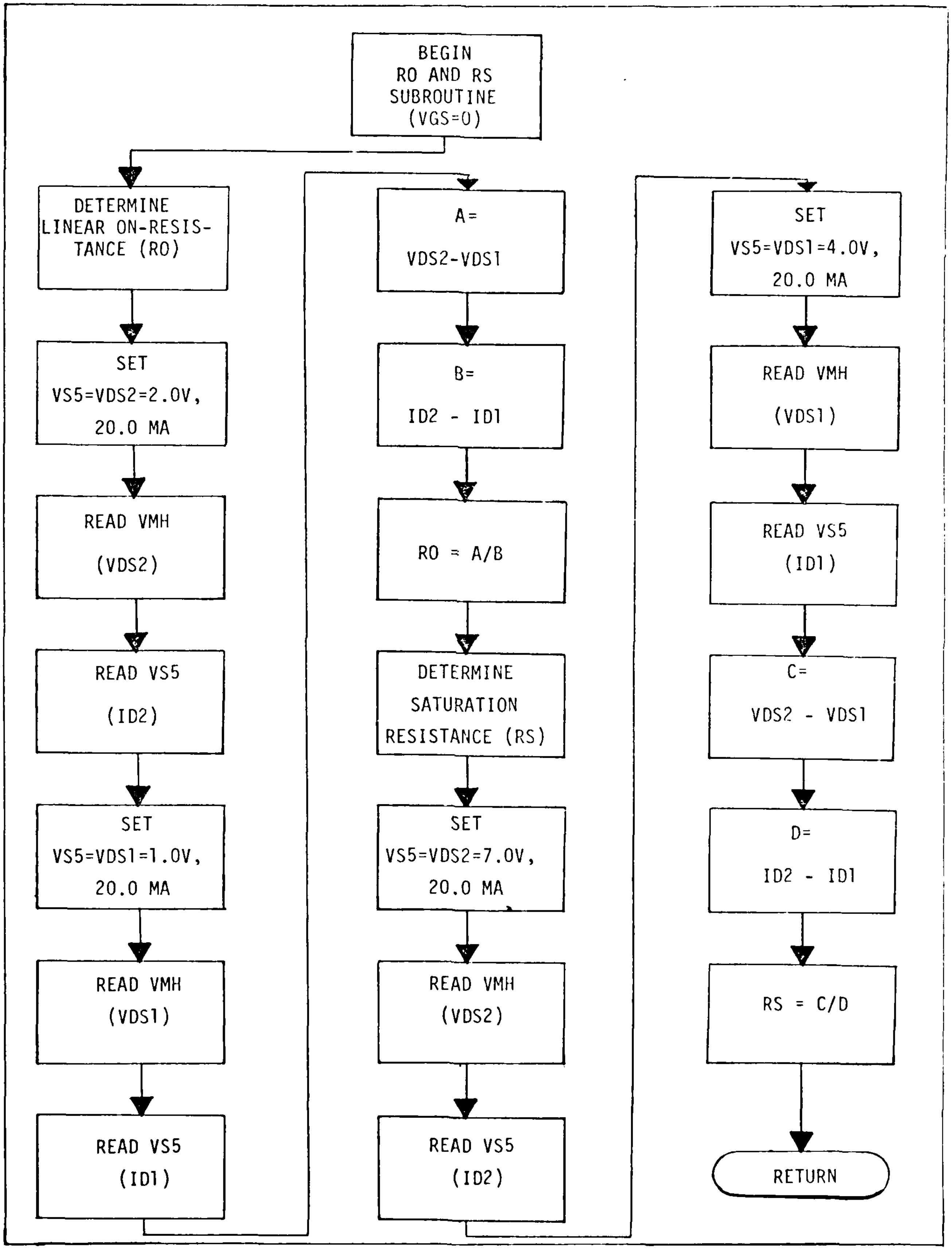


Figure 24. LINEAR ON-RESISTANCE (RO) and SATURATION RESISTANCE (RS) Measurement Subroutine Flowchart.

LIMITS Subroutine. The LIMITS subroutine was necessary in order to provide a current limit for the VP subroutine to use as a method to determine whether VP could be reached or not. In order to discuss the LIMITS subroutine, it is necessary to present the underlying rationale for its need. In the FET theory presented in Chapter II, it was pointed out that an accepted method to determine VP is to obtain ID = 1% of IDSS. The VGS voltage obtained at this ID is considered to be the pinch-off voltage, VP. In conceptualizing the method to obtain VP using the Singer tester, it was assumed that the possibility exists that a value of VP may never be reached which yields ID = 1% of IDSS, i.e., the channel may fail to pinch off due to shunt leakage or other effects. Using the 1% of IDSS method is a simple way to determine VP using a curve tracer photographs. However,the method is not a very practical one to determine VP when that value may be unknown when testing a quantity of MESFETs with no curve tracer photograph available to observe each time a test is made. Using a curve tracer each time a test was made would defeat the purpose of automated testing. Additionally, a curve tracer and the Singer tester could not be connected at the same time. Therefore, another method was considered (and eventually implemented) to determine VP.

The method used to determine VP was to expand the 1% of IDSS method to a limit. If VGS was stepped from 0.0V onward with ID measured at each step of VGS, and if ID fell within the prescribed limit, VP would have been reached. An original limit of (0.50% of IDSS) $\leq$ ID $\leq$ (1.5% of IDSS) was used, however, this was later expanded due to the decreased accuracy of the Singer caused by a problem with the current measuring equipment. This problem and a simple approach to resolve it will be presented in the results section of this chapter. The limit technique and results will also be presented then.

Another limit used to determine whether VP could be reached or not was that of a maximum allowable VGS. This value of VGS would be determined by obtaining values of VP from testing several MESFETs. A typical value of VP obtained through manually testing MESFET devices was -10.0V. This value is obviously higher than the typical -2.5V for VP obtained in Leichti's work (Ref 4:4). The VGS limit, however, can be easily changed in the MESFET program to accomodate any limit.

The approach taken in developing the very simple LIMITS subroutine was to obtain the value of IDSS measured in each device section, multiply IDSS by lower and upper limit percentages and print the limits. In addition, the voltage limits were set up as comments only and used in the VP subroutine to be discussed later. The LIMITS flowchart is shown in Figure 25. The variables ZQ (upper limit), and ZR (lower limit), were set equal to IDSS in the device section before the LIMITS subroutine was entered.

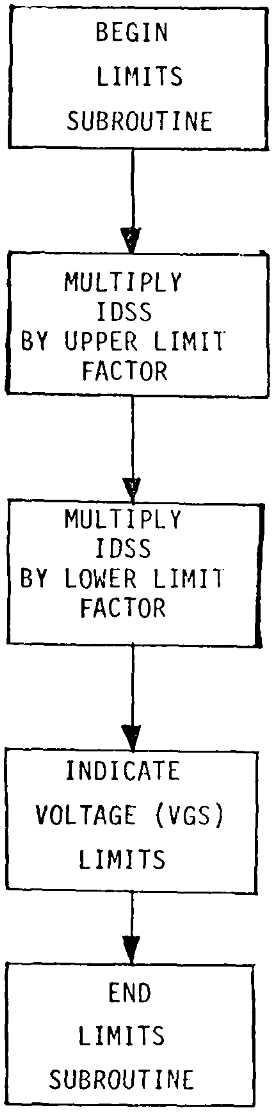


Figure 25. LIMITS Subroutine Flowchart.

Pinch-Off Voltage (VP) Subroutine. The pinch-off voltage (VP) subroutine was the most difficult to develop. Whereas the RO, RS, LIMITS, and GM subroutines involved calculations, VP involved a series of comparisons to reach a value of pinch-off. The VP subroutine can be found in Figure 26.

The objective of the VP subroutine was to determine the pinch-off voltage of the MESFET using the current limit set up in the LIMITS subroutine. The discussion of the LIMITS subroutine pointed out that the ID=1% of IDSS rule for VP may not work since the Singer may not measure ID accurately at that value. VGS would then continue stepping beyond that value of ID. Therefore, it became necessary to set up a limit.

Referring to Figure 23, it can be seen that limits of 0.5% and 1.5% of IDSS may be an approach to set up the required limit. With VGS stepped negatively and ID measured each time, ID may eventually reach a value within the required limit if the MESFET ever reaches pinch-off at all. (Obtaining currents at these low values required the high accuracy of the measuring system of the Singer tester). If the MESFET does not pinch-off, a method is required within the VP subroutine to limit the VGS voltage. This limit can be determined by obtaining maximum values of VGS for several devices. The basic idea is to determine if VGS falls within the prescribed VGS limit. If it does, ID at that value of VGS would then be subjected to the current limit. If ID falls within the limit, VP is taken at the appropriate value of VGS. If ID does not fall within the prescribed limit, VGS is then incremented by some small voltage only if VGS falls within the VGS limit. A VGS outside this limit

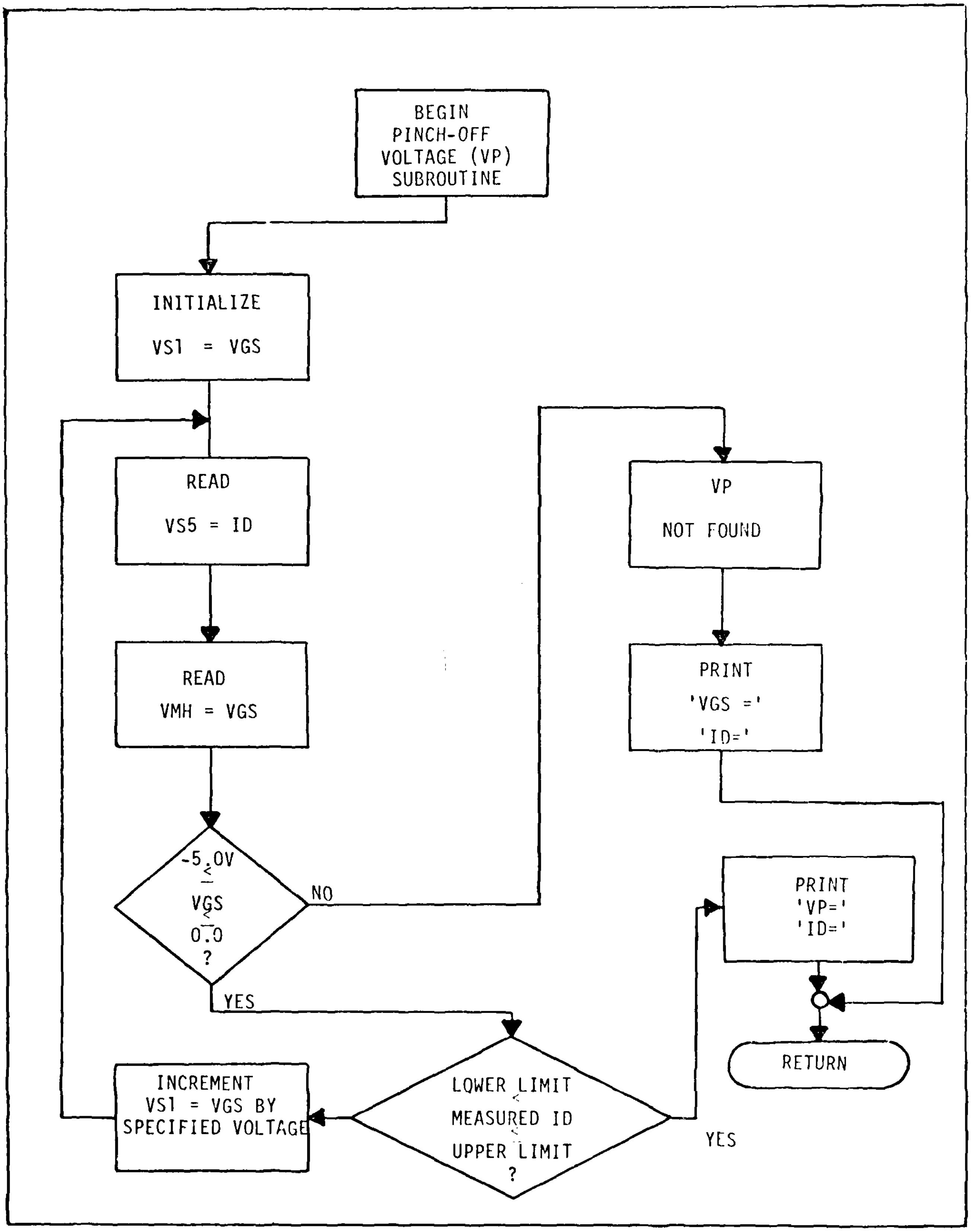


Figure 26. PINCH-OFF VOLTAGE (VP) Measurement Subroutine Flowchart.

would simply indicate that the device would never pinch-off and the subroutine would return to the main program.

Before entering the VP subroutine, items listed below must be accomplished:

1. Determine IDSS.
2. Determine limits in LIMITS subroutine.
3. Connect VS5 to drain of MESFET.
4. Connect VS1 between gate and source of MESFET.
5. Determine initial VGS and incremental or step value of VGS.

An algorithm and flowchart (important information only) for the VP subroutine follow:

1. Initialize VS1 to an initial value of VGS.
2. Measure ID.
3. Measure VGS.
4. Does VGS fall within a limit of, say, 0.0 and 5.0 volts?
5. If so, VP may not have been reached yet-therefore go to 19. If not, VGS exceeds the limit and VP cannot be reached-therefore go to 11.
6. Does the measured ID meet the conditions as specified in the LIMITS subroutine?
7. If so, VP has been reached-therefore go to 15. If not, VP has not been reached yet-therefore continue.
8. Print 'VGS=1.
9. Print 'LOWER LIMIT < MEASURED ID < UPPER LIMIT?
10. Go to 19: Continue incrementing VGS.
11. Print 'VP CANNOT BE REACHED'.

12. Print 'VGS='.

13. Print 'ID='.

14. Go to 18: Return to main program.

15. Print 'PINCH-OFF VOLTAGE (VP) = '.

16. Print 'PINCH-OFF VOLTAGE (VP) = '.

17. Print 'ID = '.

18. Return to main program.

19. Increment VGS by a small voltage.

20. Go to 2 and repeat process until VP can or cannot be determined.

Transconductance (GM) Subroutine

The TRANSCONDUCTANCE (GM) subroutine determines the basic gain conductance or GM of the MESFET. VDS = 5.0V will place the MESFET in the saturation region with VS1 initially set to 0.0V. Prior to entering the subroutine, the system is reset and then further conditioned in each device section. A discussion of the subroutine can be described in the TRANSCONDUCTANCE (GM) flowchart in Figure 28. GM results are found in the results section of this chapter.

The TRANSCONDUCTANCE (GM) will determine GM on the Singer performing the following calculations using Figure 27 as a reference:

$$GM1 = (ID4-ID3)/(VGS4-VGS3) \tag{25}$$

$$GM2 = (ID3-ID2)/(VGS3-VGS2) \tag{26}$$

$$GM3 = (ID2-ID1)/(VGS2-VGS1) \tag{27}$$

$$GM = (GM1+GM2+GM3)/3.0 \tag{28}$$

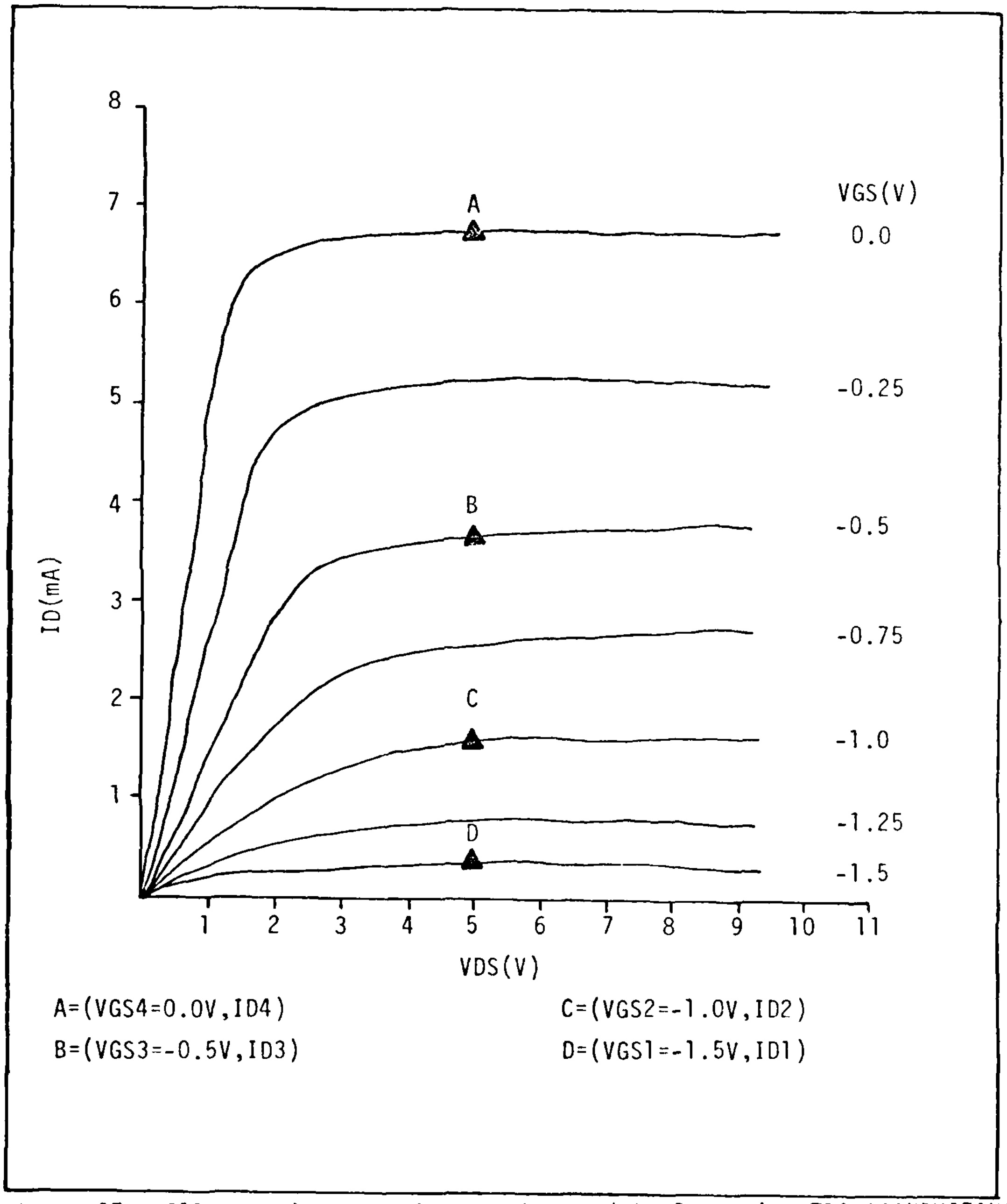


Figure 27. Illustration of Points to be used to Determine TRANSCONDUCTANCE (GM) Using the Singer Tester.

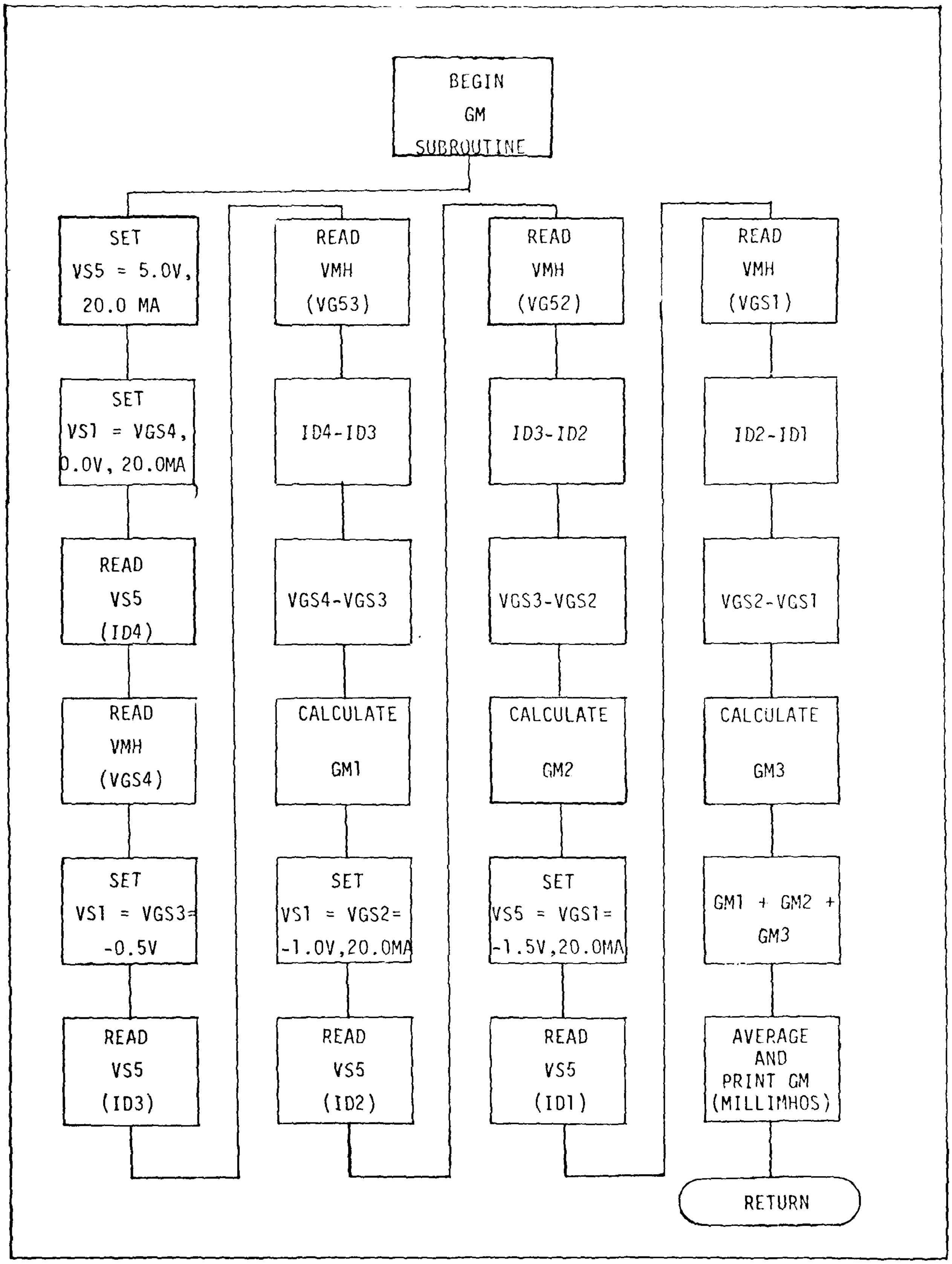


Figure 28. TRANSCONDUCTANCE (GM) Measurement Subroutine Flowchart.

BREAKDOWN VOLTAGE (BV) Subroutine. The BREAKDOWN VOLTAGE (BV) subroutine was developed to determine the breakdown voltage (BV) of a MESFET at VGS=0.0V. A practical approach (which is highly dependent on the current measuring accuracy of the Singer) is to determine BV based on a major change in the slope in the saturation region. A visual description as shown in Figure 29 will aid in the discussion of the BV subroutine flowchart, as well as an algorithm as shown below.

a. Connect VS5 and voltmeter across drain and source of MESFET.

b. Ground gate unless MESFET is the ACTIVE LOAD. BREAKDOWN VOLTAGE (BV) Algorithm:

1. Initialize VS5 = VDS1 at 5.0V; ZV = 0.5; ZF = 2.0
2. Measure ID1 (n=1).
3. Measure VDS1 = 5.0V.
4. Increment VS5 by 1.0V (VS5 = VDS2 = 6.0V)
5. Measure ID2 (n=2).
6. Measure VDS2.
7. Slope(1)=(VDS2-VDS1)/(ID2-ID1)=:Store Slope(1) at n=2.
8. Increment VS5 by 1.0V (VS5 = VDS3. = 7.0V)
9. Measure ID3 (n=3).
10. Measure VDS3 = 7.0V
11. Slope (2) = (VDS3-VDS2)/(ID2-ID1) : Store Slope (2) at n=3.
12. Is Slope (2) greater than Slope (1) by more than 1000.0? If so, BV = VDS3 = 7.0V. If not, continue
13. Increment VS5 by 1.0V. (VS5 = VDS4 = 8.0V)

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THE AUTOMATED DC PARAMETER TESTING OF GAAS MESFETS USING THE SI--ETC(U)
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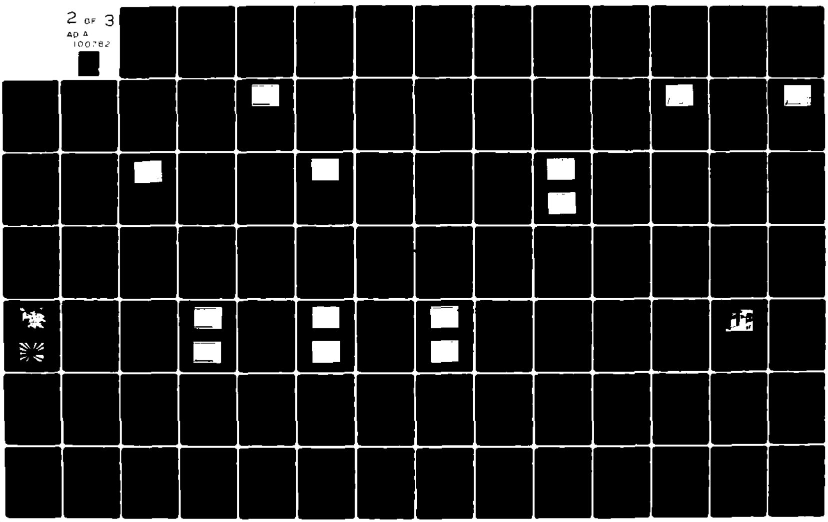

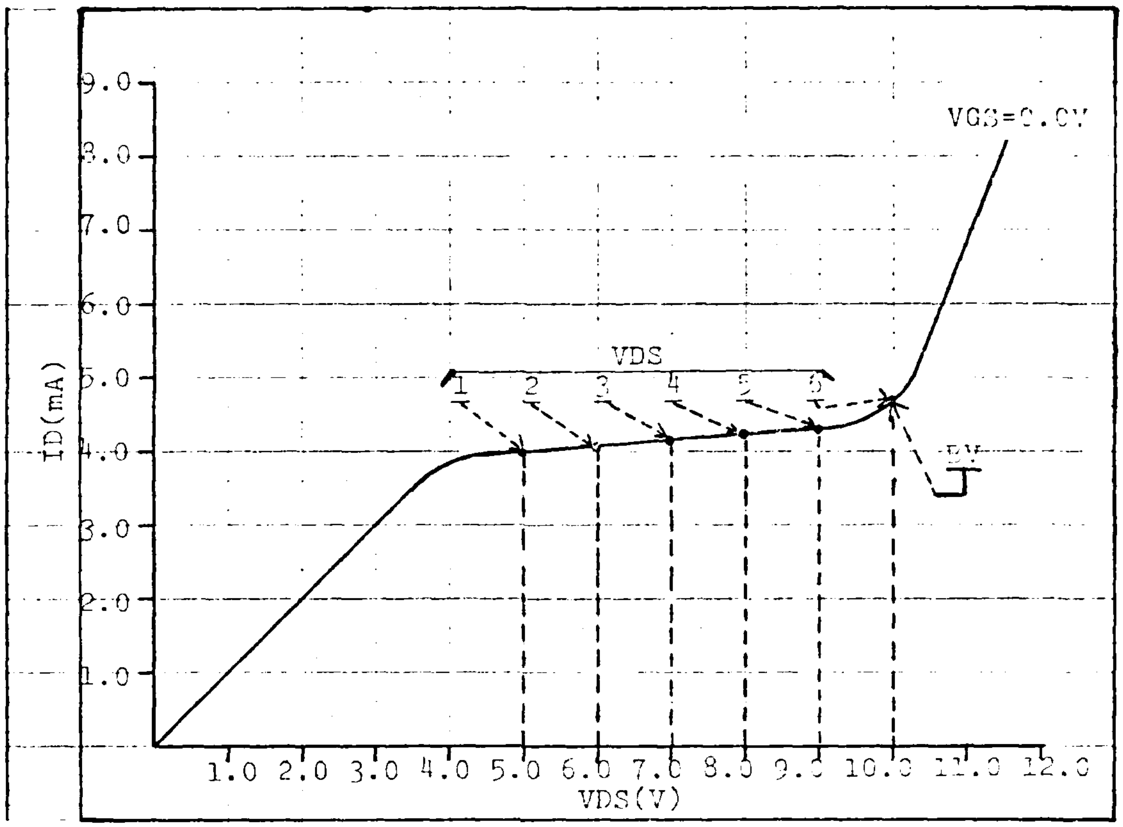

Figure 29. Illustration of Method to Determine BREAKDOWN VOLTAGE (BV) at VGS=0.0V on the Singer.

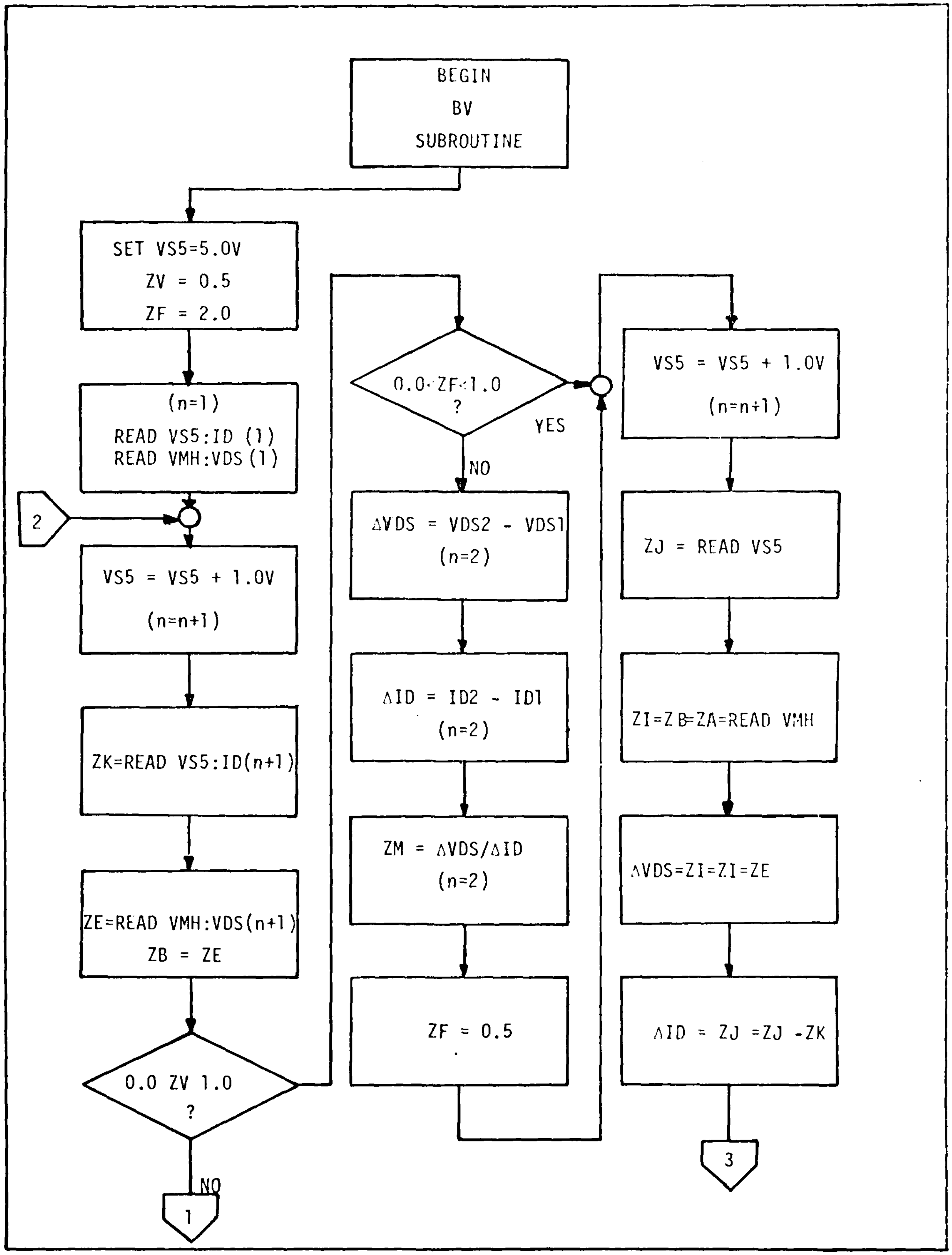

Figure 30. Breakdown Voltage (BV) Measurement Subroutine.

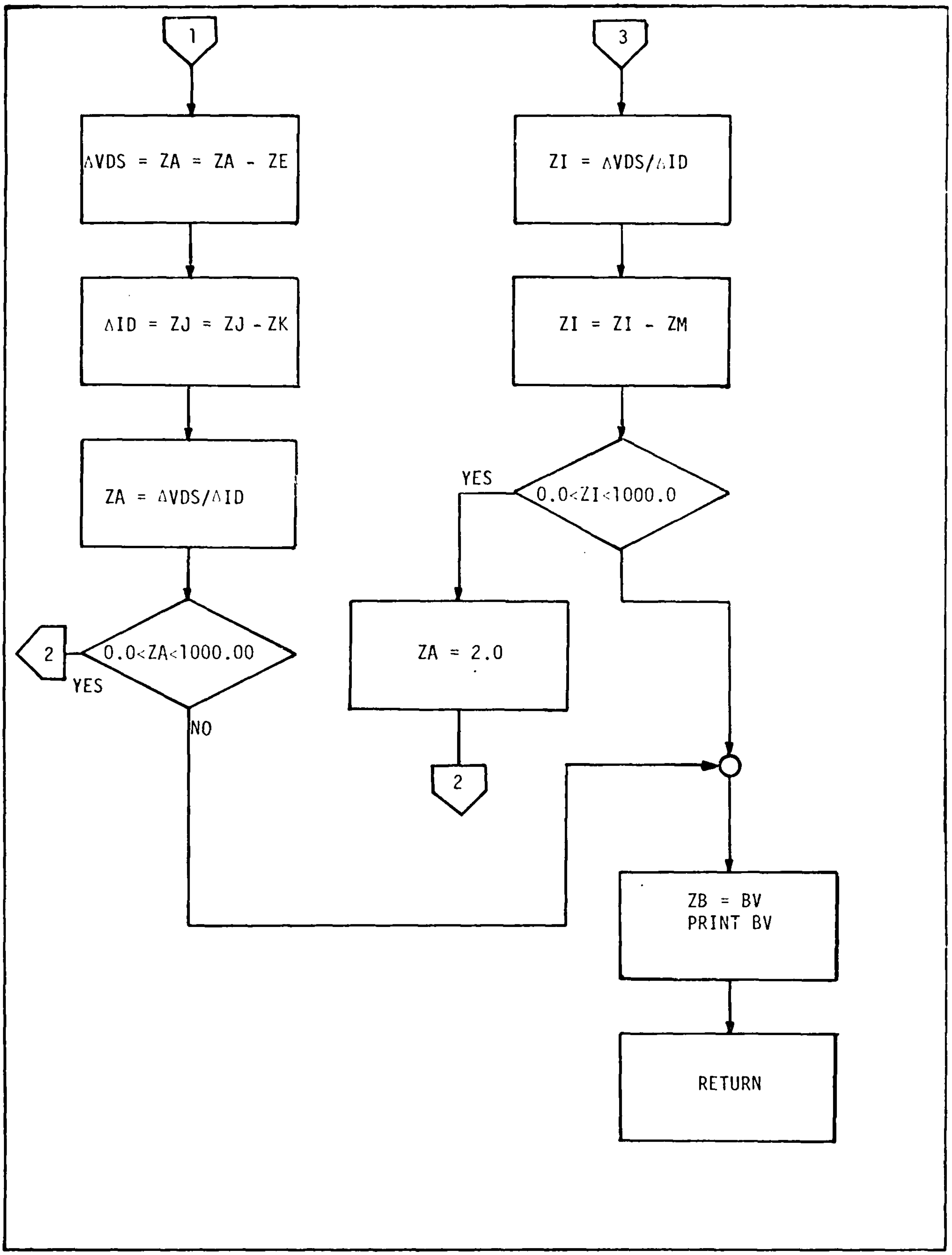

Figure 30. Continued.

14. Measure ID4 (n=4).

15. Measure VDS4 = 8.0V.

16. Slope (3) = (VDS4-VDS3)/(ID4-ID3): Store Slope (3) at n=4.

17. Is slope (3) greater than slope (2) by more than 1000.0? If so, BV=VDS4 = 8.0V. If not, continue.

18. Increment VS5 by 1.0V (VS5 = VDS5 = 9.0V).

19. Measure ID5 (n=5).

20. Measure VDS5 = 9.0V).

21. Slope (4) = (VDS5-VDS4)/(ID5-ID4): Store Slope (4) at n=5.

22. Is Slope (4) greater than Slope (3) by more than 1000.0? If so, BV = VDS5 = 9.0V. If not, continue.

23. Increment VS5 by 1.0V (VS5 = VDS6 = 10.0V).

24. Measure ID6 (n=6).

25. Measure VDS6 = 10.0V.

26. Slope (5) = (VDS6-VDS5)/(ID6-ID5): store Slope (6) at n=4.

27. Is Slope (5) greater than slope (4) by 1000.0? If so, BV = VDS6 = 10.0V. If not, continue.

It seems, a priori, that the BV subroutine in theory is a valid approach to determine the breakdown voltage of a MESFET on the Singer.

<u>SINGLE GATE and DUAL GATE DC Parameter Measurement</u>. The DC parameters to be tested in the SINGLE GATE and DUAL GATE (Figure 1) device sections are VDS, IDSS, RO, RS, VP, GM, and BV. In order to test the devices separately, one of them must be pinched-off before the other can be tested. At pinch-off device ideally represents an open circuit. Therefore, a VP must be assumed for one of the devices. A simplified algorithm is shown below:

1. Assume VP = -3.0V for DUAL GATE.
2. Pinch-off SINGLE GATE using VP program.
3. Remove -3.0V from DUAL GATE.
4. Test DUAL GATE DC parameters.
5. Keep DUAL GATE at VP and remove VP from SINGLE GATE.
6. Test SINGLE GATE DC Parameters.

In the above algorithm, the DUAL GATE is set at an assumed VP of -3.0V and is considered to be an open circuit as indicated above. VP for the SINGLE GATE is then determined. Pinch-off at an assumed -3.0V is then removed from the DUAL GATE. The DC parameters for the DUAL GATE are then tested. Afterward, the DUAL GATE is kept at VP and then VP is removed from the SINGLE GATE. The SINGLE GATE's DC parameters are then tested (except VP). Figure 31 is the flowchart for the SINGLE GATE and DUAL GATE DC Parameter measurement and is self-explanatory.

The main problem that may be encountered in testing the two gates is that the assumed VP for the DUAL GATE may not be correct. VP may actually be higher or lower than -3.0V. No special provision has been developed to reset VP if a higher value turns out to be needed. It may be necessary to study

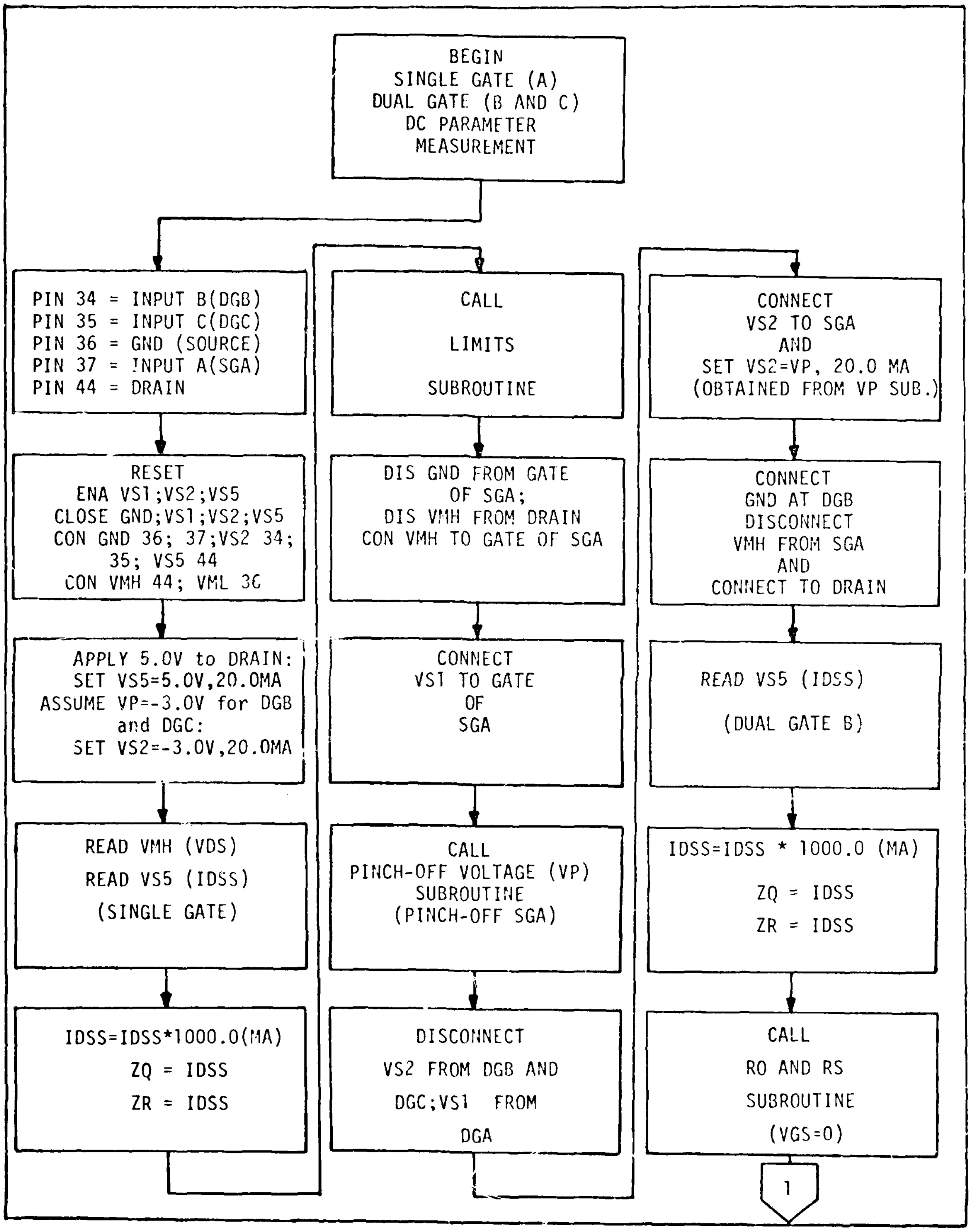

Figure 31. SINGLE GATE (A) and DUAL GATE (B and C) DC Parameter Measurement Flowchart.

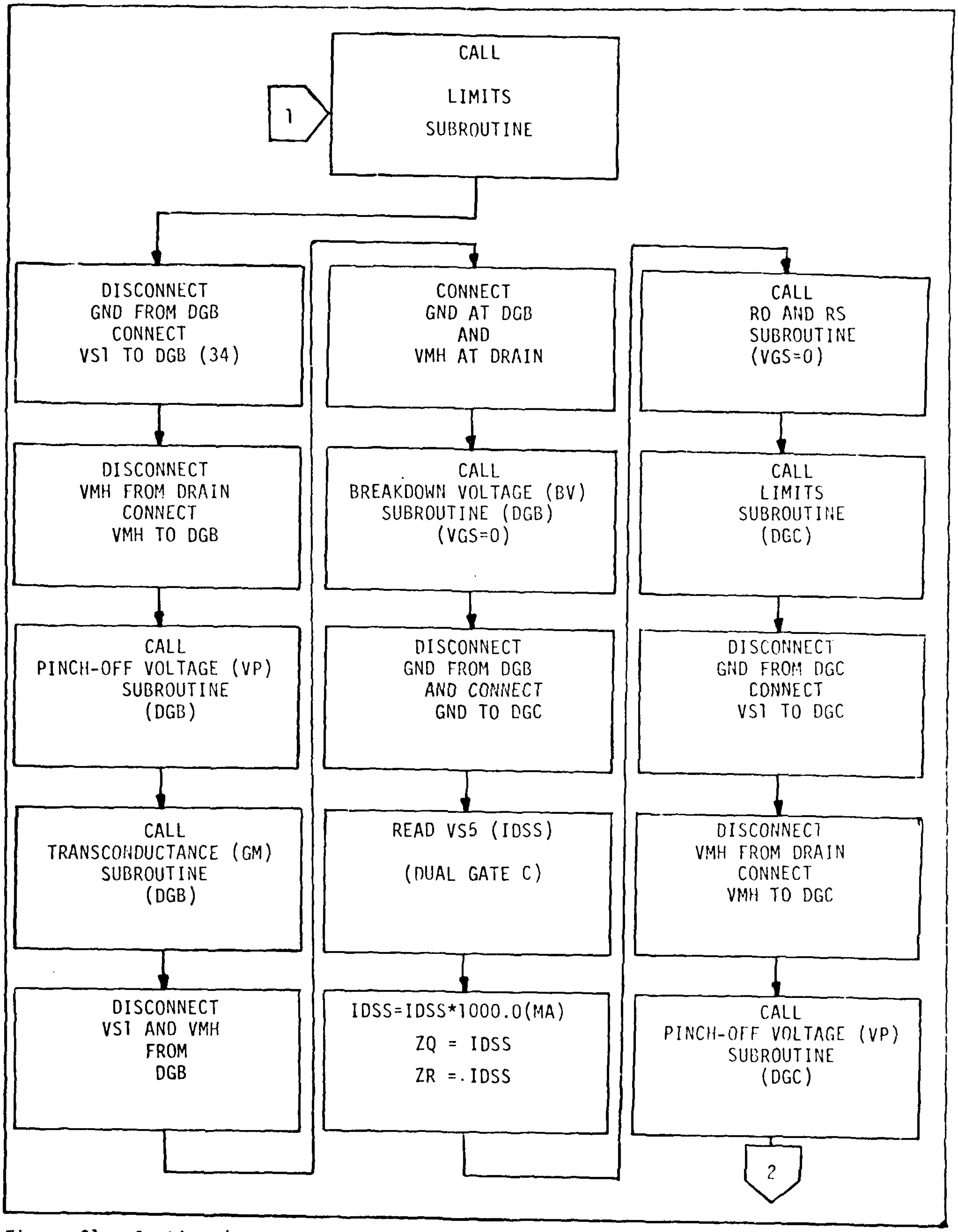

Figure 31. Continued.

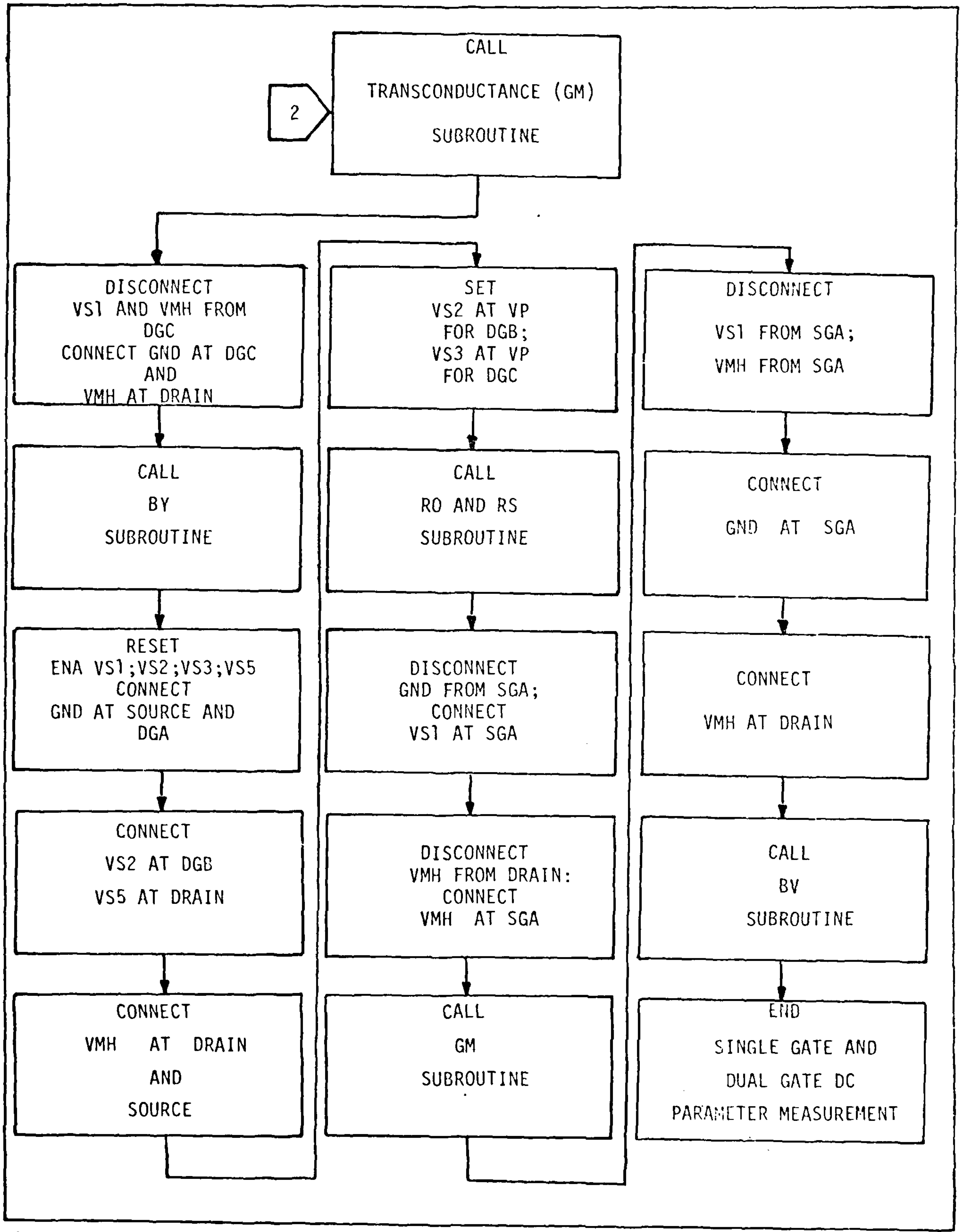

Figure 31. Continued.

several dual gate devices using the curve tracer to obtain an idea of what value of VP is needed.

DIODE DC Parameter Measurement. The DIODE device section was written to measure the forward threshold voltage (VF) and reverse threshold voltage (VR) of the three series Schottky diodes in Figure 19. An understanding of DIODE can be obtained from Figure 32 which illustrates the basic scheme used to determine VF and VR using the Singer. A flowchart for DIODE and the system connections for determining VF and VR are shown in Figure 33. Since DIODE was not actually tested, the currents indicated in Figure 32 are subject to change after required experimentation and analysis with the Singer and a curve tracer are carried out. DIODE will now be explained.

According to DIODE, VF can be obtained by applying VS5 and the voltmeter across the diodes as shown in Figure 34(a). Using conventional diode theory, VF is determined at the point where current I begins to flow after V is increased to some value. Since I and V are variable from circuit to circuit, a method to determine VF using the Singer is necessary. A limit such as $0.5 \leq I \leq 1.0$ mA was chosen (subject to change) to determine VF. V is to be increased by some amount until I falls within the set limit. When this occurs, the value of V is taken to be VF. The same method applies to VR except the current limit is $-1.0 \leq I \leq 2.0$ mA which is subject to change after experimentation with the Singer and a curve tracer. The curve tracer could be used as way to determine the actual VR or VF in order to validate DIODE.

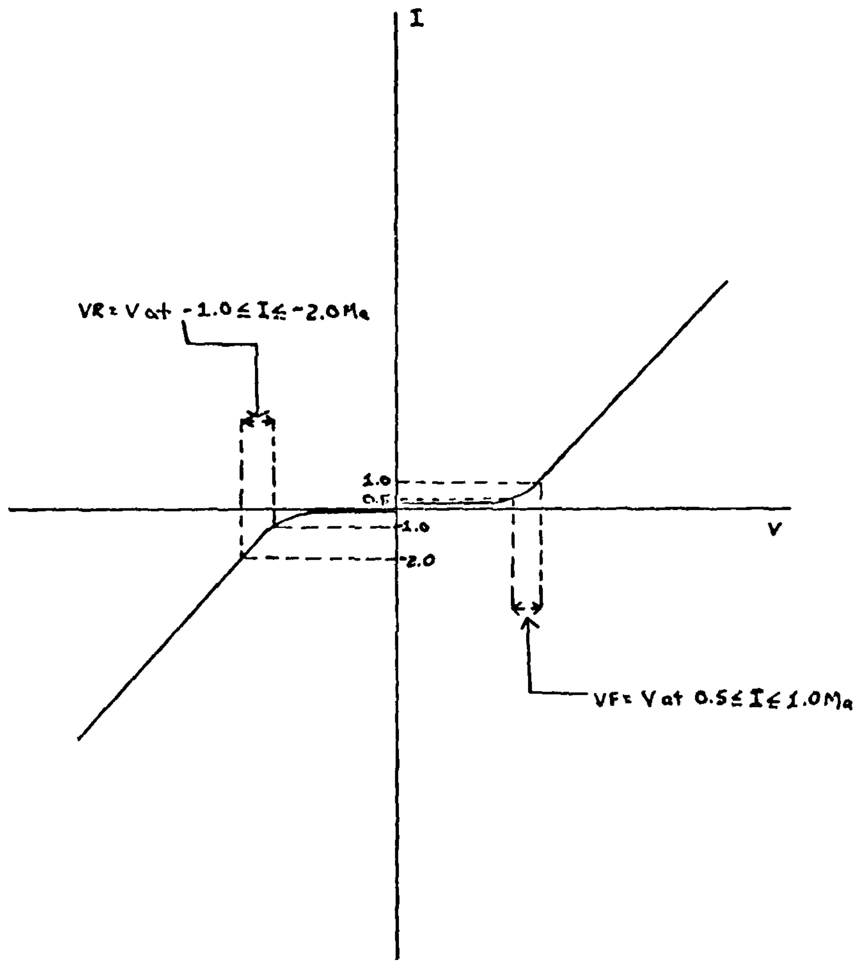

Figure 32. Illustration of Current Limits to Determine VF and VR on the Singer.

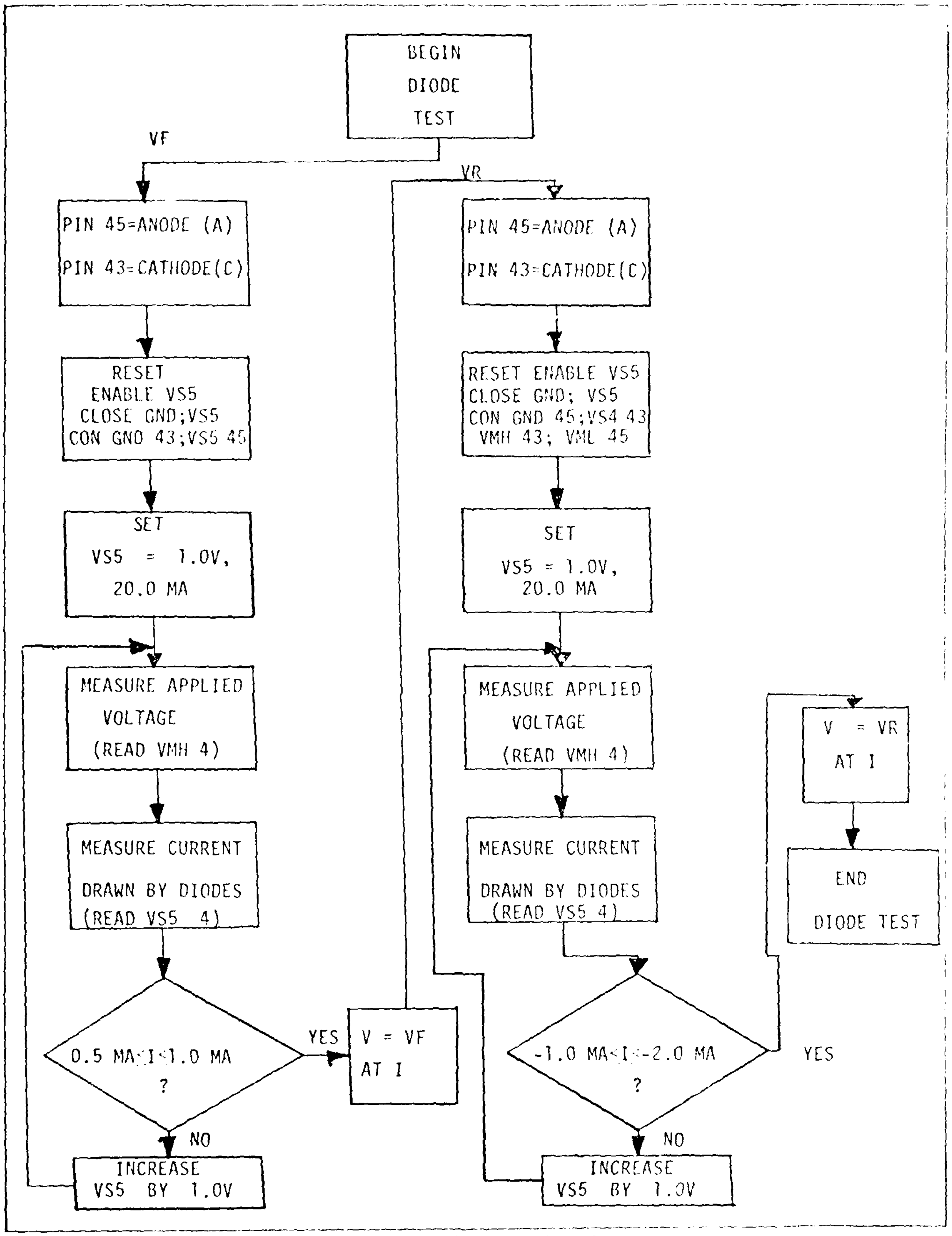

Figure 33. DIODE Flowchart to Test VF and VP on the Singer.

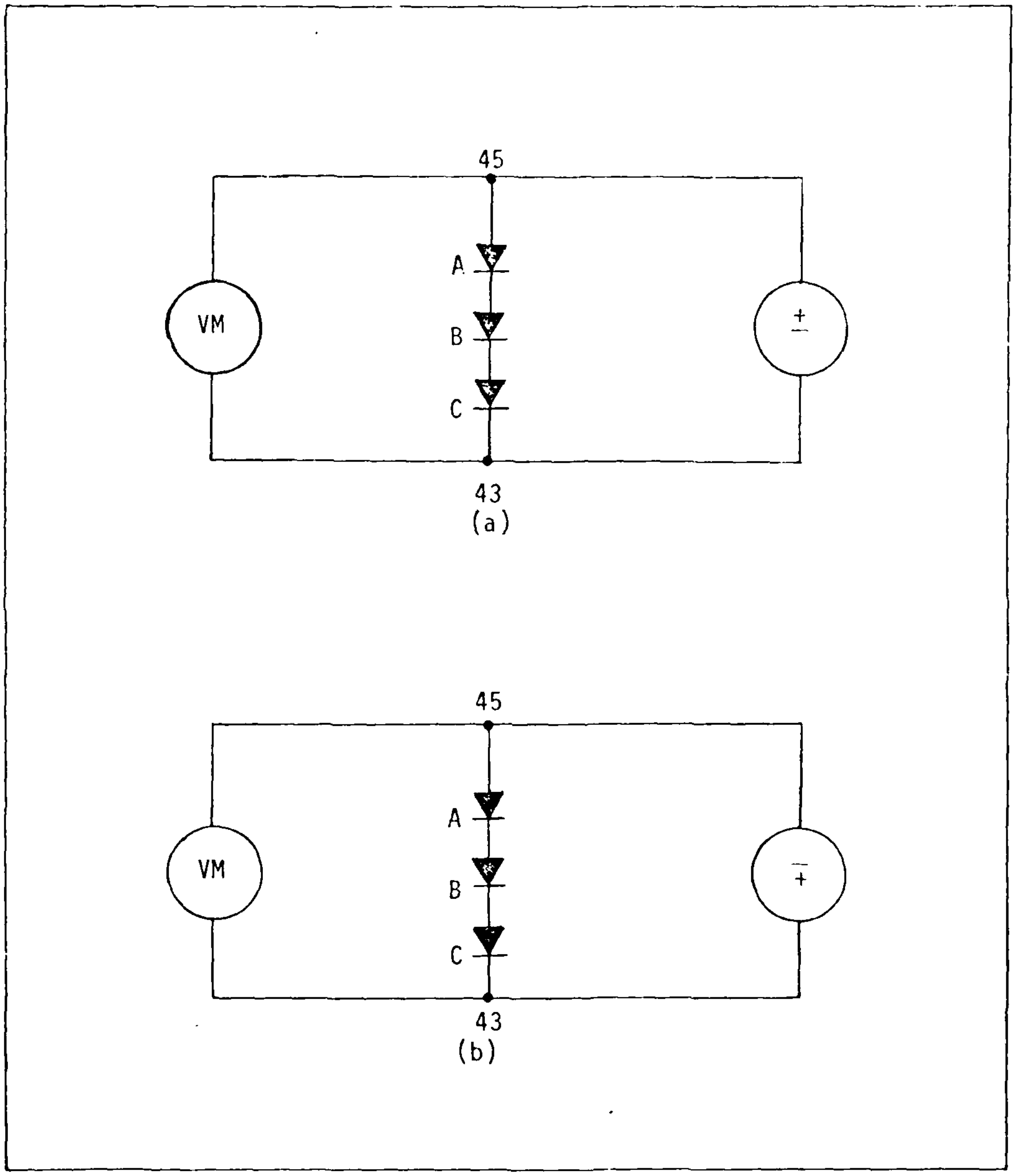

Figure 34. Required Singer Connections to Determine VF and VR. (a) Forward Threshold Voltage Connection. (b) Reverse Threshold Voltage Connection.

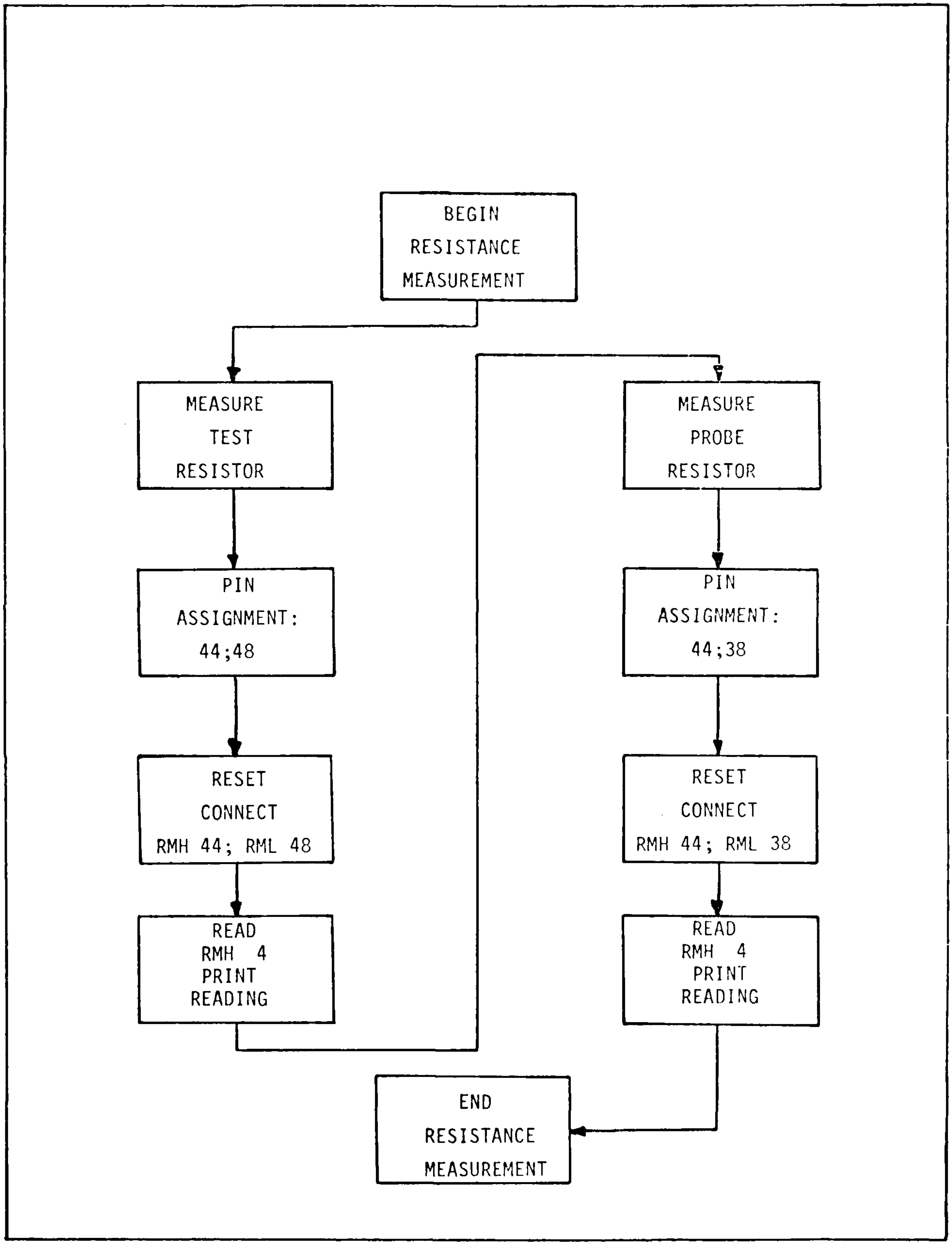

Figure 35. TEST and PROBE RESISTOR Measurement Flowchart.

TEST and PROBE RESISTOR Measurement. A method to test the resistance values of the TEST and PROBE RESISTOR is presented in Figure 35. The Singer tester is capable of directly measuring the resistance of discrete as well as integrated resistors. The implemented program of the flowchart of Figure 35 is presented in the MESFET program, Appendix I.

Summary

The algorithms and flowcharts presented in this chapter were developed to automatically test the DC parameters of the devices shown in Figure 19. The considerations made prior to the development of the actual MESFET program (Appendix I) were discussed as well as the test and programming techniques used. In the next chapter, results obtained from the automated testing of the DC parameters of Figure 19 as well as the problems encountered will be presented.

V. DC PARAMETER MEASUREMENT RESULTS AND ANALYSIS

The purpose of this chapter is to present the DC parameter results obtained through automated testing of devices of the NAND/NOR circuit of Figure 17 using the Singer automated tester. The results were obtained through application of the algorithms and flowcharts presented in Chapter IV and then converted to a coded program as shown in Appendix I.

In order to provide a means to verify the validity of the results obtained with the Singer, a Tektronix Model 576 curve tracer oscilloscope was used. The steps used to perform testing are presented in Appendix H. Values of I_D, obtained at $V_{DS} = 5.0V$ with V_{GS} as an input voltage, were extrapolated from the curve tracer photograph. These results will be presented in the form of transfer characteristic curves for comparison with the values of I_D at $V_{DS} = 5.0V$ with V_{GS} as an input voltage using the Singer.

The original strategy in the developmental stage of testing the MESFETs in the MESFET program was to test the devices developed by AFWAL/AADE. However, since an adequate quality of working devices was not available and since experimental testing involved possibly destroying these expensive devices (at the wafer level, constant probing of the devices was necessary) a decision was made to validate the program using another device. The device chosen was a packaged, n-channel, commercial silicon JFET whose DC operating characteristics were similar to those of the MESFET. This device was easier to test (since the JFET was packaged, no probes had to be used), and had the advantage that obtaining pinch-off was assured.

This strategy minimized the necessity of constantly probing and damaging the GaAs chips and reduced the risk that the probes in the probe card might be bent out of alignment during initial program development.

After proving the validity of the MESFET program using the JFET (results are shown in the following section), tests were then conducted using the GaAs MESFET devices at the wafer level. The results obtained using the JFET will now be presented.

<u>JFET DC Parameter Measurement</u>

The Texas Instruments JFET, type 2N3819, was inserted directly in the performance board (Figure 57) using the same pins as for the SOURCE FOLLOWER. The testing was performed without the inclusion of the ability to automatically step across a wafer using the TAC probe. The Singer system was prepared (Appendix H), a curve tracer photograph of the I-V curves of the JFET obtained, and finally the SOURCE FOLLOWER portion of the MESFET program applied to test the JFET.

The JFET exhibited excellant characteristics as shown in the curve tracer photograph of its I-V family of curves, Figure 36. As can be seen, the JFET exhibited excellant linearity in the ohmic and saturation regions, including the ability to reach pinch-off. The DC parameters of the JFET were also tested on the Singer tester using the MESFET program. The results obtained for both methods are shown in Table V, and Figure 37.

From Table V, it can be seen that ID measurement errors seem to increase as VGS is increased negatively (except at

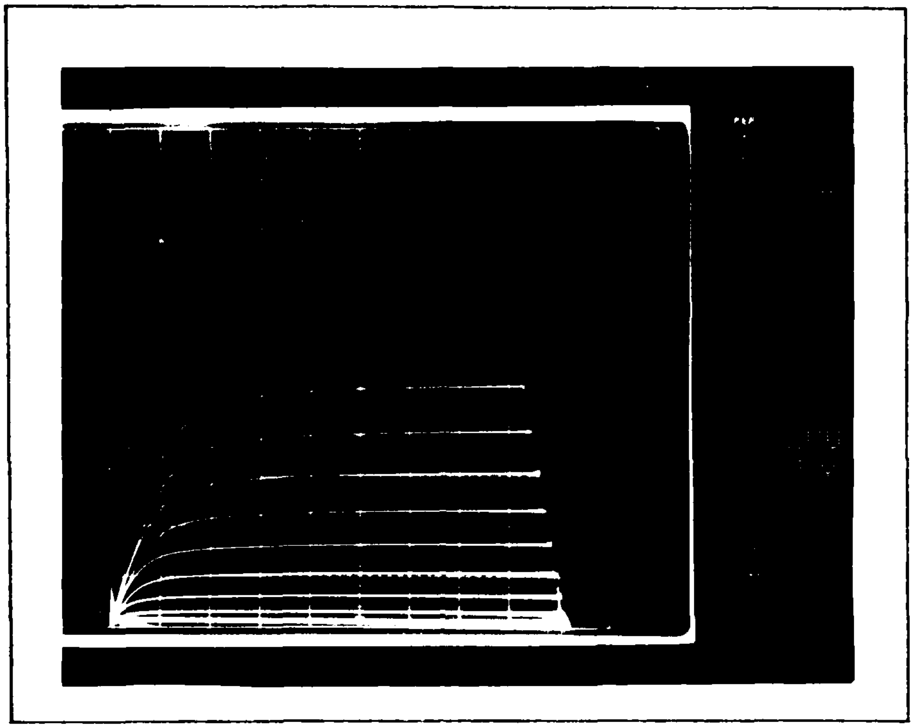

Figure 36. JFET I-V Characteristics

Table V. JFET DC Parameters

DEVICE: 2N3819 JFET			
METHOD			
DC PARAMETER	CURVE TRACER	SINGER	% ERROR
VDS(V)	5.0	4.99	0.2
IDSS(mA)	4.8	4.56	5.15
RO(Ohms)	900	987	7.9
RS(Ohms)	15,000	16,042	6.495
LIMITS	VP@1% of IDSS	0.1%≤ID≤1.1%	
VP(V)	-1.6	-1.38	16.2
ID(mA)	0.05	0.045	11.1
GM	3.07	3.65	15.97
VGS(V)	ID(mA)	ID(mA)	% Error
0.0	4.80	4.56	5.15
-0.5	2.40	2.29	4.6
-1.0	1.00	0.75	45
-1.3	0.40	0.045	788
-1.5	0.20	-----	-----
-1.6	0.05	-----	-----

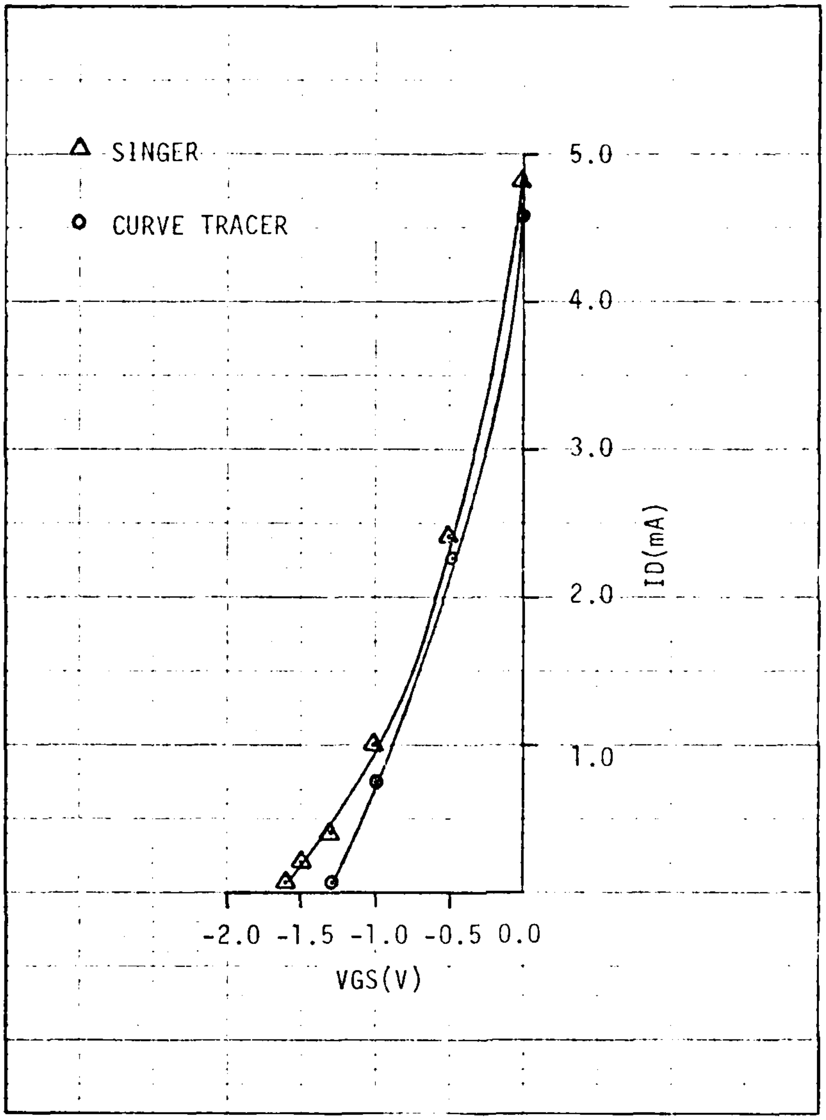

Figure 37. JFET Transfer Characteristic.

IDSS). In addition, the VP subroutine determined VP=-1.376V at ID=0.045mA. This value of ID is about 0.98% of IDSS, and is still within the indicated limits set up in the LIMITS subroutine. From the curve tracer measurement, VP=-1.6V at ID = 0.05mA which is 1.04% of IDSS. As can be seen, VP was reached at a smaller VGS on the Singer than in the curve tracer data. The VP results for the JFET, however, prove the concept that an approximate value of VP can be obtained using the limit method. With improved accuracy of the system, the actual and experimental values of ID and VP (as well as VGS), will improve in agreement.

The linear and saturation resistances are shown in the table with the indicated percentage error including the transconductance (GM) of the JFET. The techniques used to obtain these parameters were discussed in Chapters II and IV.

As pointed out above for values of ID at each VGS voltage in Table V, ID measurement errors (actual vs. experimental errors) increased as VGS increased negatively. This problem become significant as the channel of the MESFET approached pinch-off. Significant problems were later experienced with the Singer system which deserve attention. These will be presented in the next section and the method to resolve the problems will be pointed out and discussed.

Singer Tester Problems

The VP subroutine is highly dependent on the current measuring system in the Singer. A calibration program, CALIB (see Appendix H), is available on the Singer and yielded the following results for a current measurement of 1.0 ampere only, using VS5:

Sensitivity Deviation = 0.51%

Zero Offset = 0.13%

Accuracy for this particular supply below 1.0 ampere was not available and could be assumed to be much worse. However, after attempting to calibrate VS4, the possible alternate supply, it was decided not to use it due to the following characteristics at 100mA:

Sensitivity Deviation = 100%

Zero Offset = 22.03%

Sensitivity deviation and zero offset were much much worse at lower values of ID.

The problem in the current measuring capacity was believed to lie in the automatic ranging amplifier within the Singer. In the early development of the MESFET program, power supply VS1 encountered problems. The current ranging circuitry of the supply overloaded and several components were destroyed. The ranging amplifier obtains output from the supply and automatically assures that each current and voltage reading is taken at the highest gain setting to assure the most accurate results (Ref 21). Following the VS1 failure, it was assumed that when a READ command was encountered, more current beyond the specified output current was read, and this in turn reduced the capability of the ranging amplifier to produce accurate measurements. It was felt that the problem could be cured by shipping the amplifier back to the manufacturer for repair, but this could have taken weeks. The decision was made to calibrate VS5 further to provide more accuracy, but this did not seem to be sufficient. The VS1 ranging circuitry was repaired but the accuracy was reduced significantly. The board was then replaced entirely, but this did not solve the current measuring problem.

Throughout the testing of the JFET (and later the MESFET) an attempt was made to develop a method to resolve the accuracy problem. The problem could not be removed immediately and given the urgent need to test MESFET devices, a simple method to introduce error factors into the program was conceived. This method, however, turned out to be very difficult and eventually unpredictable when more than one device was tested. The error factors were determined by obtaining curve tracer photographs of a particular MESFET's I-V curves. Later, the same MESFET was applied to the Singer tester for testing. Values of I_D at a value of VGS (in 0.1V steps) were obtained with VDS=0.5V. The same values of VGS (at VDS = 5.0V) were observed on the photograph and the value of ID at that VGS was recorded. The error factor was obtained by the following:

$$\text{ERROR FACTOR} = \text{Actual ID/Experimental ID} \qquad (29)$$

An example and further discussion is presented in Appendix L.

<u>NAND/NOR Gate DC Parameter Measurement</u>

The remainder of this chapter will be devoted to the presentation of results obtained from the testing of the GaAs MESFET circuits of Figure 19. It is recognized that the data are corrupted by the current measurement inaccuracy of the Singer system. The devices tested were the SOURCE FOLLOWER, CURRENT SOURCE, and ACTIVE LOAD. The DC parameter, BV, was not tested due to the accuracy of the equipment. The SINGLE GATE, DUAL GATE, and

DIODE devices also were not tested on the Singer due to this problem. The TEST and PROBE RESISTORS were not tested, but could be easily tested using the simple program presented in Chapter IV.

An attempt will be made to demonstrate that the MESFET program is theoretically sound. This demonstration was attempted in the JFET test, and it was hoped that, given the equipment problem, tests of the MESFET devices would also be successful. The most important and sophisticated parameter to measure was the pinch-off voltage of a device. An attempt was made to reach this point despite the current measuring error of the Singer. With the equipment problem unresolved, ID measurements made at each VGS step must be in error and in turn VP will obviously be in error. A statistical analysis of DC parameter data obtained from the tests will not be presented since the validity of the numerical results is questionable.

<u>SOURCE FOLLOWER DC Parameter Measurements</u>. Several SOURCE FOLLOWERs were tested using the curve tracer prior to testing them on the Singer. Testing the devices on the curve tracer first provided the opportunity to determine which devices would be favorable to test on the Singer. SOURCE FOLLOWERs that exhibited somewhat linear characteristics in both the saturation and ohmic regions as well as those that achieved pinch-off were selected for further Singer testing. The primary objective in the MESFET program development was to simply obtain a device that exhibited a favorable I-V curve and test it further on the Singer. Many devices' I-V curves indicated that they would never reach pinch-

off or would reach breakdown prematurely. These devices were not aggressively sought after since the VP was the most important (and difficult) parameter to obtain on the Singer.

As can be seen in Table VI, VP = -3.5V at 0.4mA was obtained using the curve tracer whereas VP could not be reached using the Singer. The indicated limit set to reach the value of VP = -3.0V at ID = 1.46787 mA demonstrates theinaccuracy of the system. It can be seen that the ID obtained is actually 10.93% of IDSS. The proper VP would have never been reached using the limit of 0.5% $\leq$ ID $\leq$ 1.5%. It is important that the same limit to test VP for every MESFET is used. If not, the purpose of testing many devices automatically would be defeated since a standard limit must be used. With the Singer's inaccuracy, it was impractical to attempt to define standard limits to obtain VP. Limits of as much as 0.5% $\leq$ ID $\leq$ 10.0% were used to test the SOURCE FOLLOWERs (as well as other MESFETs). ID reached the limit eventually, but the wrong value of VP was obtained. A limit such as the one used above is very inaccurate whereas a limit such as 0.5 $\leq$ ID $\leq$ 1.5% increases the accuracy of VP. An ID of 0.4mA (2.5% of IDSS) for VP = -3.5V was obtained using the curve tracer which was 2.5% of IDSS. It seems at this point that even if the Singer were functioning properly, standard limits would not be practical. VP(Figure 38) was achieved using the curve tracer regardless of the theoretical 1% of IDSS rule. It also seems now that this problem could be in the accuracy of the curve tracer or the device itself. The problem demonstrates that a standard limit for

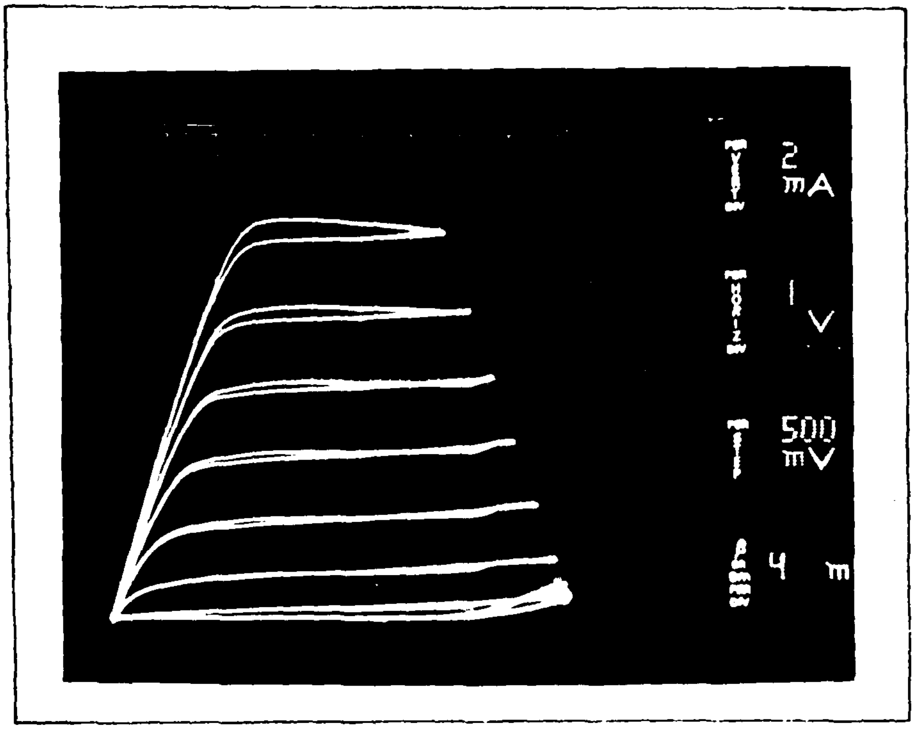

Figure 38. SOURCE FOLLOWER 'A' I-V Characteristics.

Table VI. SOURCE FOLLOWER 'A' DC PARAMETERS

DEVICE: SOURCE FOLLOWER			
	METHOD		
DC PARAMETER	CURVE TRACER	SINGER	% ERROR
VDS(V)	5.0	4.99	0.2
IDSS(mA)	16.0	16.18	1.088
RO(Ohms)	167.0	140.0	19.28
RS(Ohms)	7500.0	7375.0	1.69
LIMITS	VP@ 2.5% OF IDSS	0.5%≤ID≤1.5%	-----
VP(V)	-3.5	-3.0	16.7
ID(mA)	0.4	1.69	76.3
GM(millimho)	6.0	5.70	5.2
VGS(V)	ID(mA)	ID(mA)	% ERROR
0.0	16.0	16.18	1.088
-0.5	12.6	12.87	1.6
-1.0	9.6	9.88	2.82
-1.5	7.0	7.26	3.71
-2.0	4.4	4.95	11.17
-2.5	2.0	3.01	50.5
-3.0	0.8	1.68	52.6
-3.5	0.5	----	-----

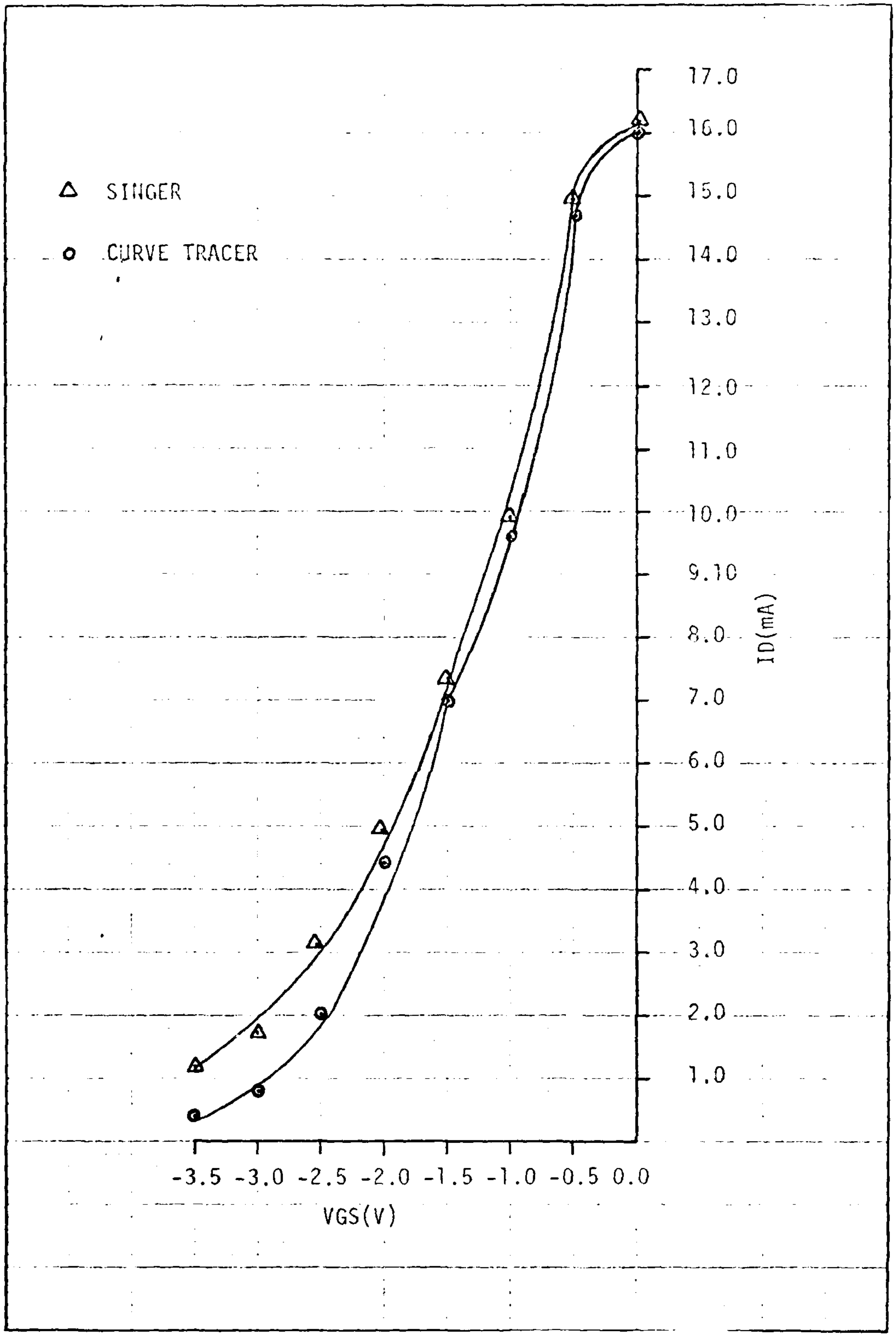

Figure 39. SOURCE FOLLOWER 'A' Transfer Characteristic.

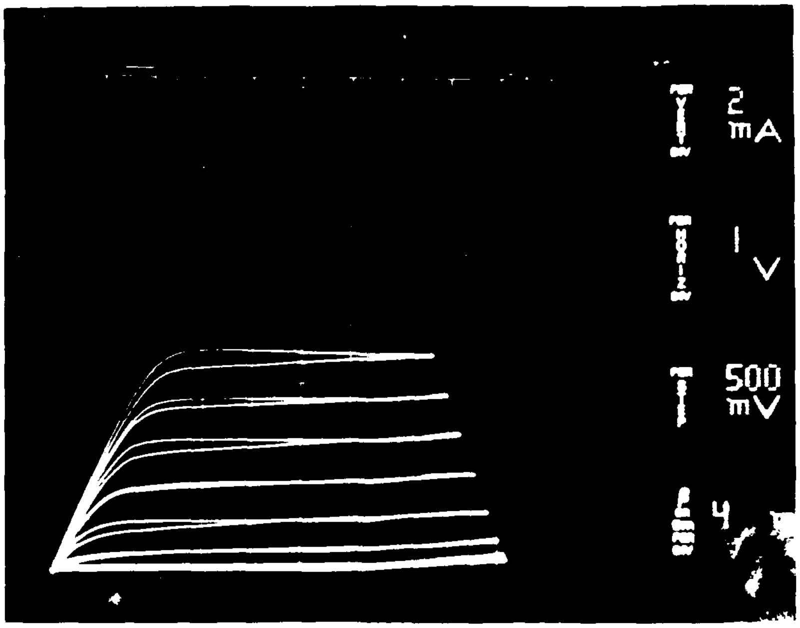

Figure 40. SOURCE FOLLOWER 'B' I-V Characteristics.

Table VII. SOURCE FOLLOWER 'B' DC PARAMETERS

DEVICE: SOURCE FOLLOWER 'B'			
METHOD			
DC PARAMETER	CURVE TRACER	SINGER	% ERROR
VDS(V)	5.0	4.99	0.2
IDSS(mA)	8.8	9.66	8.9
RO(ohms)	192.3	215.8	10.88
RS(ohms)	15,000	14,000	29.0
LIMITS	VP@ 2.27% of IDSS	0.5%≤ID≤1.5%	-----
VP(V)	-3.5	----	-----
ID(mA)	0.2	----	-----
GM(millimhos)	3.47	3.12	11.2
VGS(V)	ID(mA)	ID(mA)	% ERROR
0.0	9.0	9.66	6.85
-0.5	7.2	7.70	6.58
-1.0	5.4	6.44	16.15
-1.5	3.8	4.61	17.7
-2.0	2.2	3.27	32.75
-2.5	1.0	2.16	53.75
-3.0	0.4	1.50	73.40
-3.5	0.2	1.29	84.57

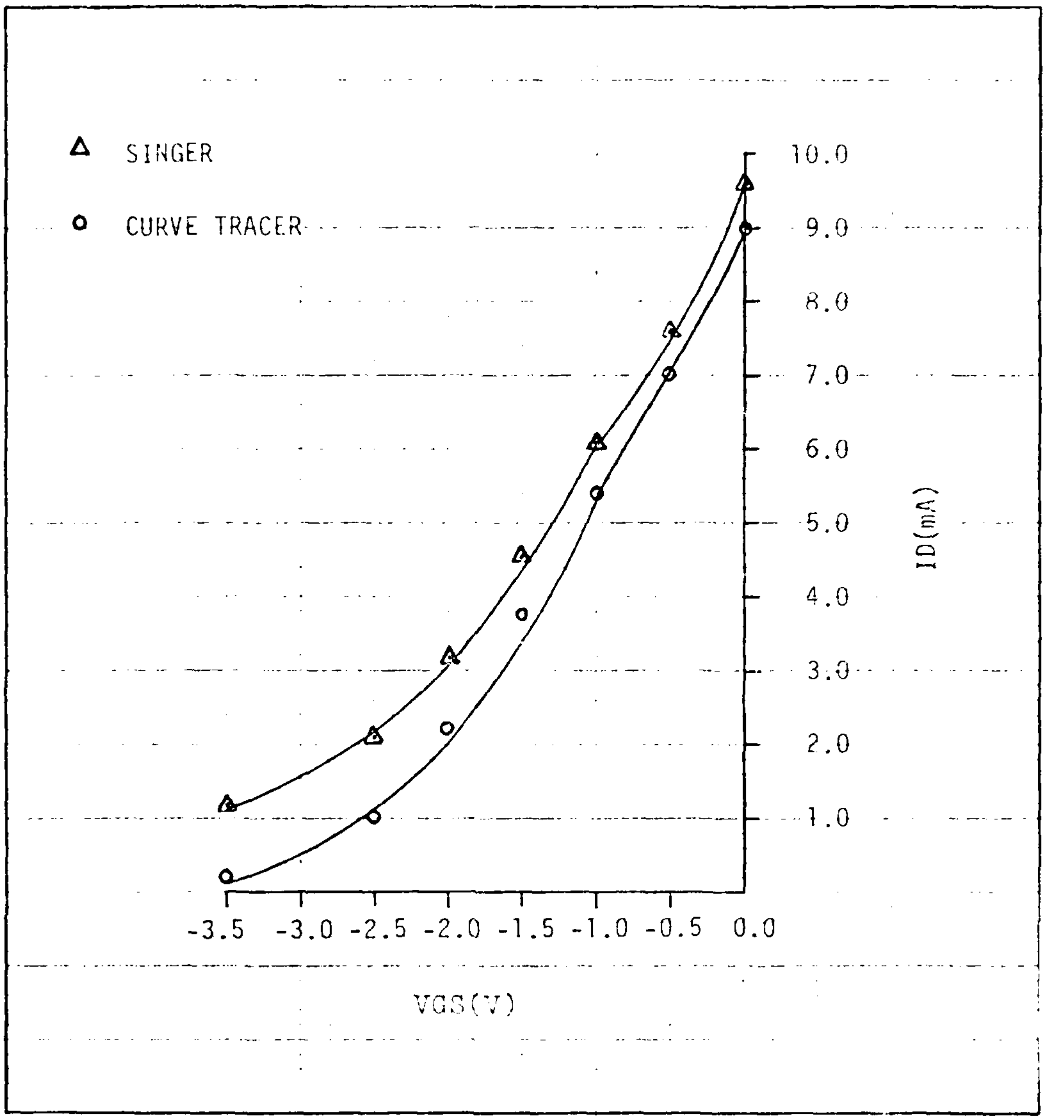

Figure 41. SOURCE FOLLOWER 'B' Transfer Characteristic.

determining VP would be difficult to obtain on the Singer with accuracy in current measurement and even more so without the accuracy.

Other parameters depicting SOURCE FOLLOWER 'A' can be seen in the table. Figure 39 depicts VGS versus ID. The figure indicates that the Singer shows some accuracy at high currents, but is low at low currents toward pinch-off. A percentage error in the table indicates the accuracy problem as ID is decreased.

SOURCE FOLLOWER 'B' results are shown in Table VII and in Figures 40 and 41. The limit was set at 0.5% ID 1.5% for the Singer. Id never reached within the set limit and therefore VP was not obtained. The program simply bypassed the expected VP. The value of ID at VGS = -3.5V is 1.29610mA at 13.4% of IDSS. This indicates that the standard limit would not apply with the Singer's accuracy. Figure 41 depicts VGS versus ID with the percentage error indicated in Table VII including other measured parameters.

CURRENT SOURCE DC Parameter Measurement

A CURRENT SOURCE was tested using the Singer tester with the results shown in Table VIII. The I-V characteristics of the MESFET as measured on the curve tracer are shown in Figure 42.

As can be seen in the table, the percentage error varies somewhat and does not show consistency as ID decreases. A graphical representation can be seen in the transfer characteristics of the CURRENT SOURCE as shown in Figure 44.

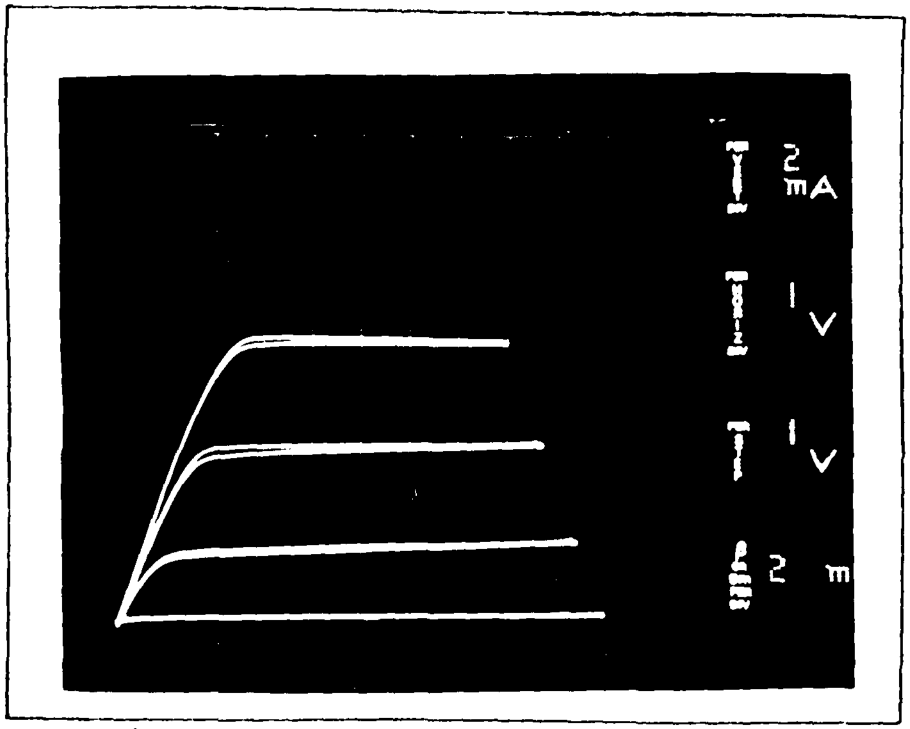

Figure 42. Current Source I-V Characteristics.

Table VIII. CURRENT SOURCE DC Parameters.

DEVICE: CURRENT SOURCE			
	METHOD		
DC PARAMETER	CURVE TRACER	SINGER	%ERROR
VDS(V)	5.0	4.99	0.2
IDSS(mA)	11.6	14.29	18.2
RO(ohms)	166	182	9.6
RS(ohms)	7500	4525	39.7
VP(V)	3.0	-----	----
ID(mA)	0.6	-----	----
GM(millimhos)	3.7	4.451	16.8
Limits	VP@ 3.9% of IDSS	0.5%≤ID≤1.5%	----
VGS(V)	ID(mA)	ID(mA)	%ERROR
-0.0	11.6	14.29	
-0.5	9.0	11.4	21.0
-1.0	7.0	8.80	20.45
-1.5	5.0	6.38	21.6
-2.0	3.0	4.27	29.7
-2.5	1.6	1.62	1.20
-3.0	0.6	1.38	56.5

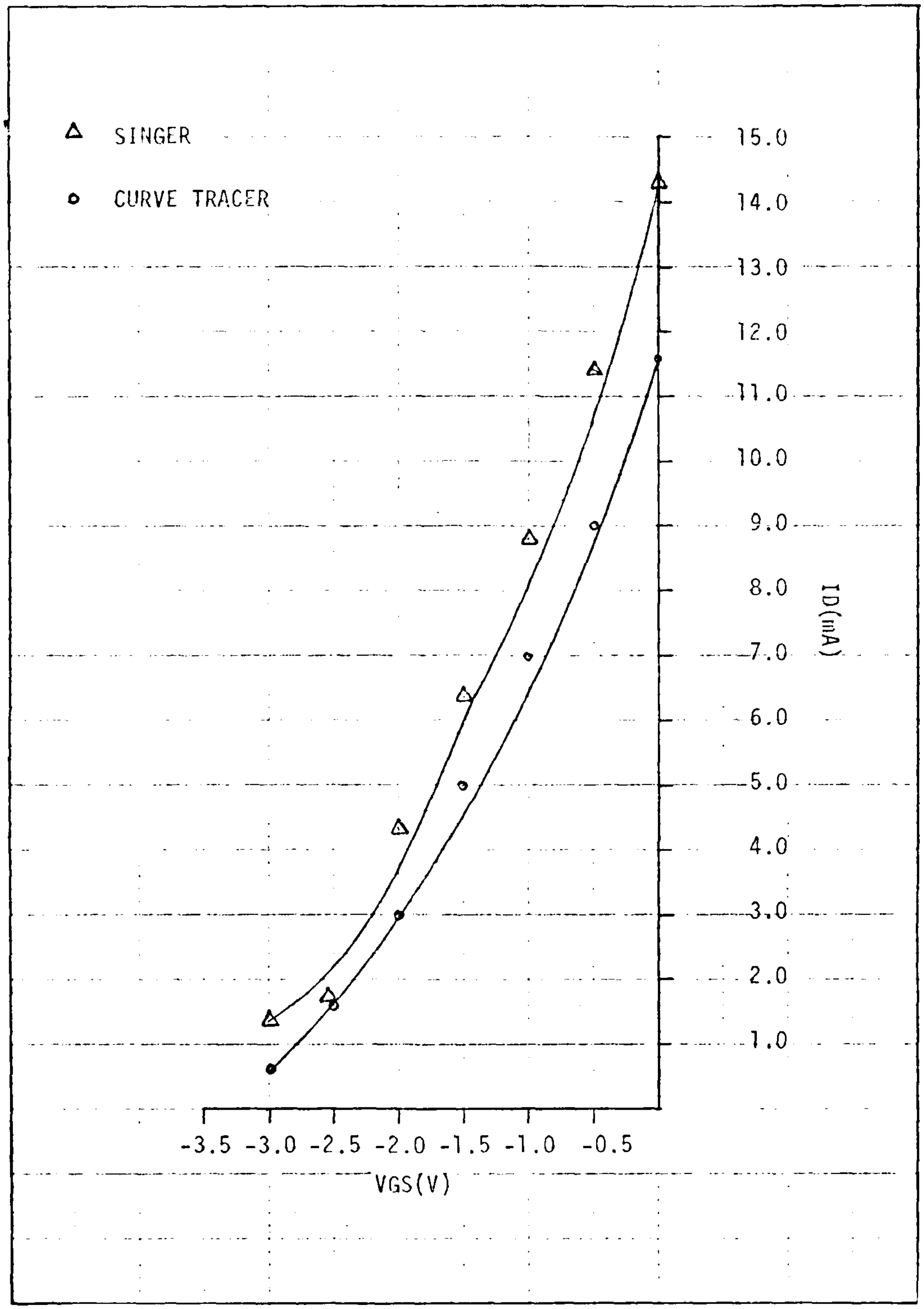

Figure 43. CURRENT SOURCE Transfer Characteristic.

ACTIVE LOAD DC Parameter Measurement

An ACTIVE LOAD was tested with the results shown in Table IX. The I-V characteristics of the MESFET as measured on the curve tracer are shown in Figure 44. Since the source of the ACTIVE LOAD is shorted to its gate, VP nor GM can be tested.

Summary

In this chapter results obtained through the automated testing of the MESFETs of Figure 19 were compared to those measurement results using a curve tracer. The results from testing the devices were not as successful as expected due to the current measuring inaccuracy of the Singer. As a result of this problem, it was felt that continued testing of the SINGLE GATE, DUAL GATE, and DIODE programs as well as the BREAKDOWN VOLTAGE subroutine would not yield significant results. The TEST and PROBE RESISTORS were not tested, but should not be difficult to test if the program presented in Chapter IV is used. It is hoped that with the Singer tester's accuracy problem removed, better results will be obtained.

Chapter VI will now be devoted to discussing the capabilities and limitations of the Singer tester. A simple system design to provide the Singer with a dynamic testing capability is also presented.

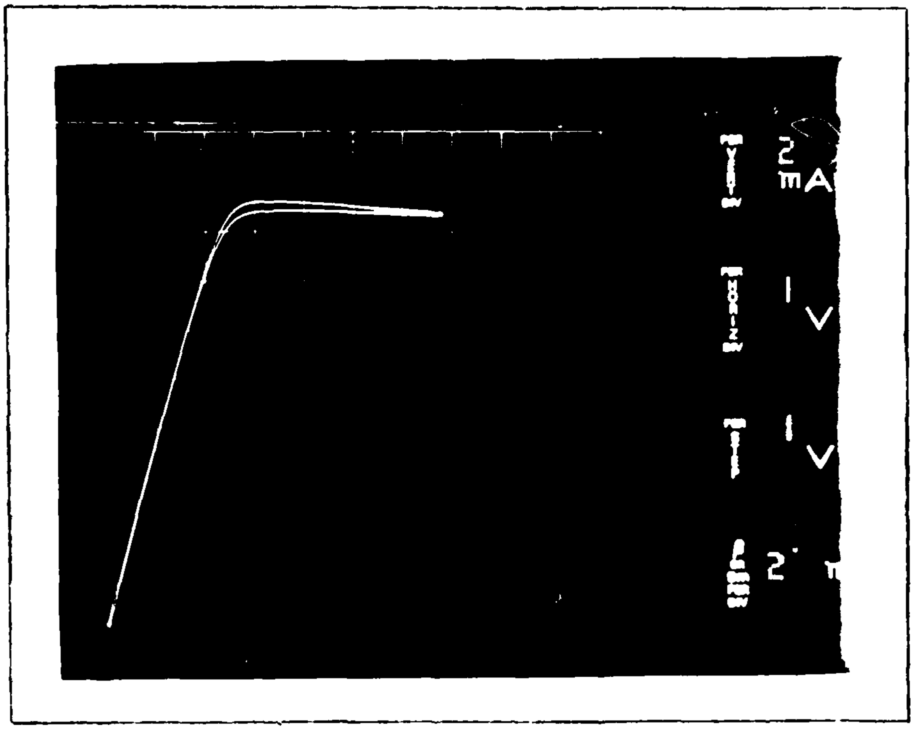

Figure 44. ACTIVE LOAD I-V Characteristics.

Table IX. ACTIVE LOAD DC Parameters

DEVICE: ACTIVE LOAD			
	METHOD		
DC PARAMETER	CURVE TRACER	SINGER	% ERROR
VDS(V)	5.0	4.99	0.2
IDSS(mA)	17.0	20.0	15.0
RO(ohms)	156	172	9.3
RS(ohms)	7500	4500	40.0

VI. CAPABILITIES AND LIMITATIONS OF THE SINGER TESTER

In the previous two chapters, procedures to test the DC parameters of an JFET and MESFET using the Singer tester were developed and measurements obtained for most of these parameters. An attempt was made to prove that the Singer was capable of testing the static DC parameters of a JFET and MESFET. This capability had never been proven before. The results obtained were not spectular since the Singer encountered measurement accuracy problems. With an improved measurement accuracy, a better idea of the Singer's capability in the area of JFET/ MESFET DC parameter testing will be obtained.

The purpose of this chapter is to study the capabilities and limitations of the Singer tester. These will be determined by information published in the Singer manual (Ref 21), tests conducted to study the voltage output characteristics of the Singer and the principle results of the testing of the MESFET (Chapter V) and the4-bit accumulator (Appendix J).

Published Specifications of the Singer Tester

According to the preliminary draft written by Singer for the tester (Ref 21), the system is capable of performing full DC parametric testing, data plotting, data logging, and data analysis on semiconductor circuits (integrated and discrete) as well as resistors (integrated and discrete). These tests can be performed at the wafer level using the TAC Automatic Probe Unit (See Appendices C and G) or at the packaged circuit level. Packaged circuits can be directly inserted in the system's performance board. Singer developed the tester for the initial purpose of testing transistors, integrated circuits and resistors. The Singer tester has the capability to perform DC measurements on the devices indicated below.

Bipolar Transistors. The following DC parameters can be measured on the Singer:

A. H_{FE}(small-signal current gain) as a function of I_B (typical I_B = 100μA to 100mA).

B. H_{FE} as a function of I_c (typical I_c = 100μA to 100mA).

C. V_{BE} as a function of I_E (typical I_E = 10μA to 10mA).

D. BV_{EBO} (typical 0 to 10V, 0 to 1mA, with independently adjustable voltage and current limits).

E. BV_{CBO} (typical 0 to 100V, 0 to 1mA, with independently adjustable voltage and current limits).

F. BV_{CEO} (typical 0 to 32V, 0 to 1mA, with independently adjustable voltage and current limits).

G. BV_{CES} (typical 0 to 32V, 0 to 1mA, with independently adjustable voltage and current limits).

H. BV_{DS} (typical 0 to 100V, 0 to 1mA, with independently adjustable voltage and current limits).

I. $V_{CS(sat)}$ as a function of I_c (100μA to 100mA).

J. I_{CBO} as a function of V_{CBO} (typical 100μA from 0 to 12V).

K. I_{CS} as a function of V_{CS} (Typical 100pA from 0 to 32V).

L. I_{EBO} as a function of V_{EBO} (typical 100pA from 0 to 6V).

Integrated Circuits. The following DC parameters for medium-scale integrated circuits can be measured on the Singer:

A. Input leakage currents.

B. Input level voltages.

C. Input threshold voltages.

D. Output level voltages.

E. Output fanouts.

F. Total device supply current.

G. Supply and bias voltages.

H. Supply voltage variation sensitivity.

<u>Integrated (and Discrete) Resistors.</u> The following characteristics can be determined on the Singer:

A. Absolute value of resistance (typical 10 ohms to 100k ohms).

B. Ratio between any two resistors.

For further information concerning specifications and characteristics of the Singer tester, see Appendix B.

<u>Singer Voltage Output Characteristics and High Speed Testing Capability</u>

Tests were conducted to determine the voltage output characteristics of the Singer tester. Of primary interest in the study of these characteristics is the frequency at which the Singer power supplies can be turned on and off which results in the formation of square waves. To form these square waves requires the development of a simple program to switch a supply on and off in an infinite loop. A program to obtain the output of Figure 45 is as follows.

```
100:  Program A
110   ENABLE VS5
120   CLOSE GND;  VS5
130   CON GND 40; VS5 42
140   SET VS5 0.0V, 20.0mA
```

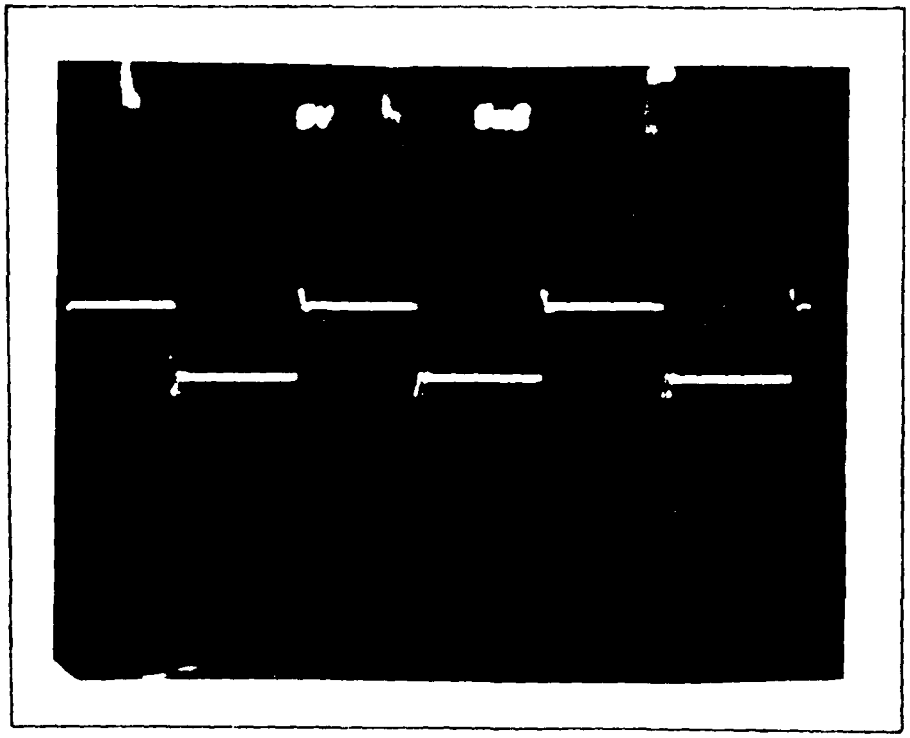

Figure 45. Program 'A' Voltage Output Characteristics.

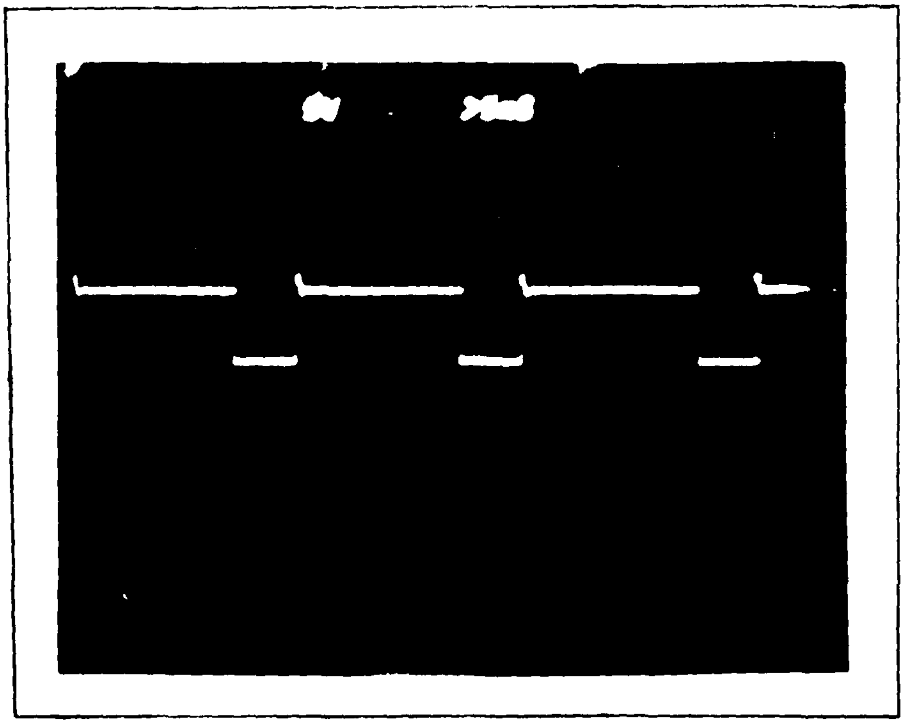

Figure 46. Program 'B' Voltage Output Characteristics.

```
150   SET VS5 5.0V, 20.0mA
160   SET VS5 0.0V, 20.0mA
170   GOTO 140
180   END
```

The program is designed to switch the VS5 power supply from 0.0V to 5.0V, back to 0.0V and then repeat the process until the programmer depresses the 'BREAK' switch on the TI Silent 700. According to Figure 45, the period of the square wave is approximately 17 mS for a frequency of 58 Hz. The output voltage square waves were obtained by connecting an oscilloscope across a 1000 ohm resistor which is in turn connected to pins 40 and 42. The amplitude of the square wave signals is 5V. The width of each square wave is approximately 9ms.

Figure 46 depicts the output of VS5 when the following program is used:

```
100:  Program 'B'
110   ENABLE VS5
120   CLOSE GND
130   CLOSE VS5
140   CON VS5 42
150   CON VS5 42
160   SET VS5 5.0V, 20.0mA
170   DIS GND 42
180   DIS VS5 40
190   GOTO 140
200   END
```

The oscilloscope was connected as before. As can be seen the period of each square wave is approximately 16mS at a frequency of 62.5 Hz, and an amplitude of 5.0V.

It is very obvious that the Singer is not capable of any form of high speed testing. To test MESFETs at the wafer level dynamically would require a signal source of 3 to 6GHz. The Singer's dynamic capability is therefore practically nonexistent.

The Singer depends directly on: the data transfer rate (direct memory access (DMA) at 275,000 words per second (Ref 23) within the Varian computer, delay over the bus between the Varian and the power supplies, and the slew rate (approximately 1 V/mS (Ref 21)) of each power supply. Additionally delay exists in commanding the matrix system to switch to the desired pins. Taking all of this into account indicates that in order to perform any type of automated high speed testing would require the use of an external signal source. Such a source would be connected to the Singer via the external instrument patch panel. The source could then be brought under computer control through required programming. The source would simply be switched on externally. A CON (CONNECT) command such as

CON EXT A 42

would simply connect the source at 'EXT A' on the patch panel to pin 42.

Due to the extremely small wavelengths at 3-5 GHz needed to dynamically test the NAND/NOR circuit of Figure 19 (unpackaged), a test fixture other than the one (probe card and TAC probe controller) used for DC parametric testing on the Singer must be used. The use of probes and the cable connection between them and the system performance board of the Singer would certainly introduce considerable delay and, of course, undesirable capacitance and inductance. In order to perform automated dynamic testing using the Singer would require a test fixture using coplanar 50 ohm transmission lines (Ref 4:35). Using this type of test fixture would require that each chip be tested separately within the fixture. This means that each chip to be tested must be diced from the wafer. Some means of measuring the output signals of the NAND/NOR circuit and recording their characteristics would be needed. Additional equipment would be needed in order to perform dynamic testing using the Singer. Figure 47 shows a simple block diagram of a proposed dynamic testing system.

Referring to Figure 47, it can be seen that via the instrument board, the Varian controls the matrix system and two tri-state buffers. As shown an appropriate signal source (for frequencies up to at least 5 GHz) is connected to the external patch panel. The output frequency of the signal source should be preset. By program control such as a CON EXT A 42 (if the signal source is connected to EXTERNAL PORT A) command, the signal source will be connected to pin 42 of the matrix system. The A input (V_{GS}) of the single gate of Figure 1(a) can be connected to pin 42 via an appropriate transmission line. The output of the single gate could then be applied (with an appropriate transmission line) to a measuring instrument. The instrument will measure the output voltage of the MESFET. The Varian, via the instrument control board would signal the tri-state buffer to output the measured voltage (the voltage should be A/D converted at the

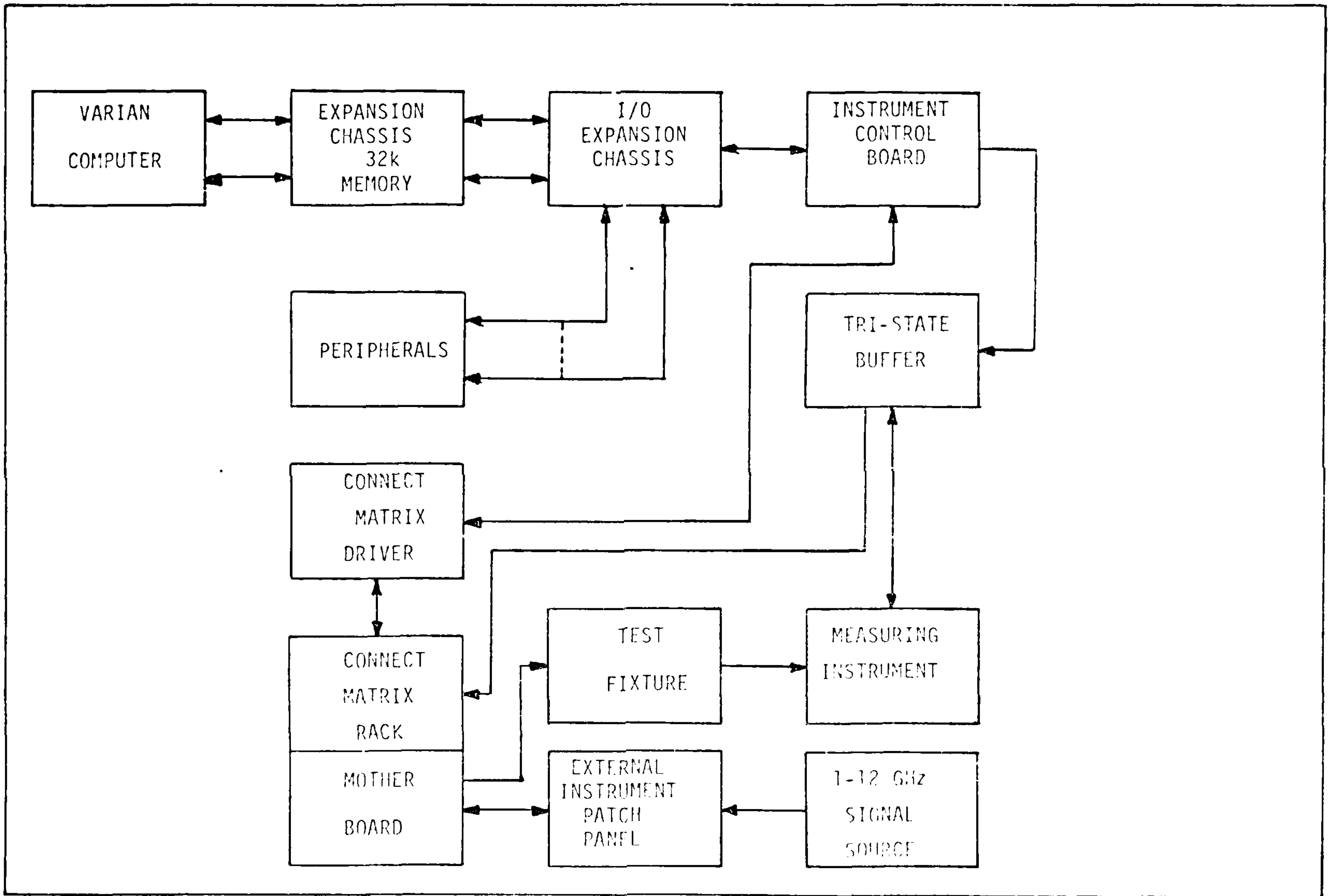

Figure 47. Proposed Dynamic Testing System Using the Singer Tester.

measuring instrument) to the matrix system. The voltage would then be transferred to the line printer or teletype upon reaching a print command. As for the magnetic tape, the voltage would be transferred to it upon the execution of a STORE Command.

It should be mentioned that the Varian may not be able to handle the rate of data obtained through the high-speed dynamic testing of GaAs MESFETs. It would therefore be necessary to add a storage buffer between the tri-state fubber and the measuring instrument.

The previous discussion of Figure 47 has been kept simple due to the many variables involved. In order to test all of the MESFETs of Figure 1(a), the text fixture must be built to provide inputs and outputs for each MESFET. The transmission lines and matrix system will certainly attenuate and delay the input signals, requiring corrections to be taken into account.

The simple design of Figure 47 is a proposed method to incorporate dynamic testing into the Singer tester. The design may be incomplete, of course, but serves as a basis for future development (beyond this thesis). It is certain that changes to the system design will be necessary.

One problem that exists with this system is the fact that a test fixture must be developed for each chip to be tested. With this situation, it seems that the goal of automatically testing a MESFET dynamically and recording the data in an efficient manner may be defeated. This is due to the fact that the Singer's primary interface for testing devices at the chip or wafer level is via a probing system such as the one used to test the DC parameters of the MESFET. Additionally, the Singer is designed to test many chips on a wafer, but to dynamically test a MESFET chip, as mentioned before, requires that each chip be tested separately. However, with the system design of Figure 47 (or a modification thereof), the capability would exist to record the dynamic test data via magnetic tape as can be done with static data. The modified Singer test system would therefore provide the capability to record data efficiently for one chip at a time. The Singer would also provide an integrated or unified capability for testing both DC and dynamic parameters.

Figure 47 indicates that output voltage measurements only can be made. With reasonable effort, a frequency measurement capability to determine propagation delay could also be designed and implemented.

Limitations of the Singer

As determined in Chapter V, the Singer, at the time of the MESFET testing, lacked the capability to measure currents as low as 0.2mA. This is due to the fact that the current measuring subsystem required extensive calibration which could not be done easily by government personnel. With the subsystem calibrated by the manufacturer and with the power supplies also calibrated, the Singer's accuracy should be improved. With this current measurement problem, proper pinch-off voltages could not obtained.

From experience through testing the 4-bit accumulator of Appendix J, it can be concluded that the Singer does not have the capability to provide more than one pulsed signal (at different sequences) at a time, at any frequency. The phase clock signals, Phase-1 and Phase-2, are examples of this limitation. This problem is due to the programming of the Singer to provide a sequence of these signals in Figure 69 as well as the power supplies' capability to provide the desired delay between each pulse. The period of each pulse is very difficult to control and may be accomplished by using DELAY commands. This method was used and poor results were obtained.

Summary

The capabilities and limitations of the Singer tester were not fully explored. Other cases may arise beyond the scope of the thesis that may reveal more information of the Singer. From the information presented, it is obvious that the Singer tester cannot dynamically test devices. The only method to provide a pulsed signal is through programming. Figure 47 provides a basic approach to add a dynamic capability to the Singer tester. In Chapter VII, conclusions derived from the experiences and results obtained through testing as well as recommendations which might lead to further investigation will be presented.

VII. CONCLUSIONS AND RECOMMENDATIONS

Conclusions

An attempt has been made to provide AFWAL/AADE the capability to automatically test the DC parameters of GaAs MESFET NAND/NOR logic circuits at the wafer level using the Singer tester. A computer program was developed based on FET theory using the Singer's available software. Results obtained through the application of the program to actual devices have been presented. It is recognized that the data obtained is inaccurate. This is a result of the Singer measuring system inaccuracies. Therefore, the reliability of the Singer is low and requires an additional effort in repairing/calibrating the measuring system (range amplifier, digital voltmeter) in order to acquire worthwhile test results.

A study of the capabilities of the Singer has been conducted. The Singer presently does not have the capability to perform dynamic testing; however, the system can be expanded to perform in this area.

A DC model of the GaAs MESFET has been proposed and evaluated for its ability to predict DC parameter data obtained using the Singer tester. An analysis of the model has been conducted with results to demonstrate the model's potential in predicting the DC parameter data.

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Recommendations

It is obvious from the previous discussion that many recommendations can be made to provide better results than those presented in the thesis. The first and foremost matter than should be resolved is to remove the current measuring inaccuracy of the Singer tester. Work has been completed in repairing and calibrating the range amplifier and A/D converter. Power supply VS5 should be calibrated so as to reduce the current measuring deviation obtained during computer controlled calibration runs. VS4 can be used instead if the calibration runs indicate the current measuring deviations to be lower than for VS5.

The pinch-off voltage subroutine, VP, should then be tested using a Source Follower or Current Source MESFET device from Figure 19. Of particular interest in this subroutine is the current limits obtained in the LIMITS subroutine. A current limit such as 0.05% of IDSS $\leq$ ID $\leq$ 1.0% of IDSS should be attempted first. It is recommended that several devices be tested using this limit. A statistical analysis of the results should be made indicating how many devices reach VP at this limit. This limit may narrow or widen depending on the results. Comparison should be made with the I-V curves obtained on a curve tracer. An extensive investigation should be made to determine a 'standard' current limit if one exists. This 'standard' limit must be applicable to all devices and cannot be changed during a test.

Secondly, the SINGLE GATE (SGA) and DUAL GATE (DGB and DGC) devices should be tested using the SINGLE GATE and DUAL GATE subprogram in the MESFET program. The subprogram has been compiled with no errors of particular importance again is the Singer's capability to pinch off either device according to the presentation made in Chapter IV. Unless pinchoff is obtained for each device, no valid results can be obtained for the other parameters of the device.

The BREAKDOWN VOLTAGE (BV) subroutine has been compiled with no errors. No results have been obtained thus far and it is recommended that a commercial JFET be used in testing initially to avoid destroying a MESFET. This subroutine should be tested after all other subroutines have been tested and statistical results have been obtained.

Primary emphasis has been placed in developing the basic precedures to test the most important DC parameters of the MESFET devices. These were IDSS, RO, RS, VP, and GM. These parameters can be measured without destroying the MESFET as could possibly be done b. esting for the breakdown voltage. Since most of the time was spent in developing and testing the previously mentioned parameters, actual testing of the DIODE, TEST, and PROBE resistors, and the SINGLE and DUAL GATE device programs were not checked out. These devices also were not tested since the Singer's measuring accuracy was low.

It is recommended that statistical results are obtained from the testing of the SOURCE FOLLOWER, CURRENT SOURCE, and ACTIVE LOAD prior to testing the diodes, resistors, single and dual gate devices. IDSS, RO, RS, VP, and GM are the most basic and important parameters. Successful testing of the SOURCE FOLLOWER, CURRENT SOURCE, and ACTIVE LOAD will provide the basic foundation for testing the SINGLE GATE and DUAL GATE devices.

In order to record the large amount of data obtained through testing hundreds of devices on a wafer, commands have to be added to the MESFET program to store data on magnetic tape. Additionally, a program must be written to read data from the tape and print it in an understandable manner.

An attempt has been made in this thesis to remedy the deficiencies initially encountered in the documentation of the Singer tester and to collect for convenient reference the information needed to use the system. The results obtained should form the basis for further development aimed at providing the full test capability needed in the GaAs logic program.

BIBLIOGRAPHY

1. Hooper, William W., and Philip L. Hower. "Design and Performance of the GaAs FET," IEEE Transactions on Solid-State Circuits, SC-5(6): 319-322 (December 1970).

2. Schockley, W. "A Unipolar Field-Effect Transistor," Proceedings of the IRE, Vol. 40: 1356-1376 (Nov. 1952).

3. Liechti, C. A. and Rory VanTuyl. GaAs Schottky-Gate Field-Effect Transistor Medium-Scale Integration. AFAL-TR-77-176. Wright-Patterson AFB, Ohio: Avionics Laboratory, 1977.

4. ______. Gallium Arsenide Digital Integrated Circuits. AFAL-TR-74-40. Wright-Patterson AFB, Ohio: Avionics Laboratory, 1974.

5. ______. GaAs Digital Integrated Circuits. AFAL-TR-76-264. Wright-Patterson AFB, Ohio: Avionics Laboratory, 1977.

6. Liechti, C. A. "Microwave Field-Effect Transistors-1976" IEEE Transactions on Microwave Theory and Techniques, MTT-24(6): 279-300 (June 1976).

7. Liechti, C. A. and Rory VanTuyl. "Gallium Arsenide Spawns Speed," IEEE Spectrum: 41-47 (March 1977).

8. Liechti, C. A. "Performance of Dual-Gate GaAs MESFETs" as Gain-Controlled Low-Noise Amplifiers and High-Speed Modulators," IEEE Transactions on Microwave Theory and Techniques, MTT-25(6): 461-469 (June 1975).

9. Yang, Edward S., Fundamentals of Semiconductor Devices. New York: McGraw-Hill Book Company, 1978.

10. Drangeid, K. E. and R. Summerholder. "Dynamic Performance of Schottky-Barrier Field-Effect Transistors," IBM Journal of Research and Development, 14(2): 82-94 (March 1970).

11. Millman, Jacob and Christos C. Holkias. Integrated Electronics: Analog and Digital Circuits and Systems. New York: McGraw-Hill Book Company, 1972.

12. Mulvey, John. Semiconductor Device Measurements. Beaverton, Oregon: Tektronix, Incorporated, 1968.

13. Wallmark, J. and H. Johnson. Field-Effect Transistors: Physics, Technology, and Applications. Englewood Cliffs, New Jersey: Prentice-Hall, Incorporated, 1966.

14. Liechti, C. A. and Rory VanTuyl. "GaAs MESFET Logic with 4-Ghz Clock Rate," IEEE Journal of Solid-State Circuits, SC-12(5): 485-596 (October 1977).

15. Cutler, Philip, Solid-State Device Theory. New York: McGraw-Hill Book Company, 1972.

16. Barlev, A. Semiconductor and Electronic Devices. New York: John Wiley and Sons, 1969.

17. Sze, S. M. Physics of Semiconductor Devices. New York: John Wiley and Sons, 1969.

18. Shur, Michael S. "Analytical Model of GaAs MESFETs," IEEE Transactions on Electron Devices, ED-25(6): 612-618 (June 1978).

19. Hower, P.L., et al. "The GaAs Field-Effect Transistor," Semiconductors and Semimetals, Vol. 7A, New York: Academic Press, 1971.

20. Furutsuka, Takashi. "GaAs Dual-Gate MESFETs," IEEE Transactions on Electron Devices, ED-25(6): 580-586 (June 1978).

21. Singer Automatic Integrated Circuit Test System User's Manual. Glendale, CA: Singer Corp., 1972.

22. Automatic Integrated Circuit Test System Programming Manual. Glendale, CA: Singer Corp., 1972.

23. Varian 620 Training Manual. Irvine, CA: Varian Data Machines, 1972.

24. VORTEX Reference Manual. Irvine, CA: Varian Data Machines, 1972.

25. Ruch, Jacques G. "Electron Dynamics in Short Channel Field-Effect Transistors, "IEEE Transactions on Electron Devices, ED-19: 652-654 (June 1972).

26. Gray, Paul E., et al. Electronic Principles, Physics, Models and Circuits. New York: John Wiley and Sons, Inc., 1966.

27. Liechti, C.A. And R. B. Larrick. "Performance of GaAs MESFETs at Low Temperatures," IEEE Transactions on Microwave Theory and Techniques: 376-381 (June 1976).

28. Pucel, R. A. and D. Masse'. "Performance of GaAs MESFET Mixers at X Band," IEEE Transactions on Microwave Theory and Techniques, MTT-24(6): 351-360 (June 1976).

29. Statz, H., et al. "Noise Characteristics of Gallium Arsenide FETs," IEEE Transactions on Electron Devices, ED-21: 549-562 (September 1974).

30. Eden, R. C. "GaAs FET Digital Integrated Circuits," IEEE Transactions on Electron Devices, ED-24: 1209-1210 (September 1977).

APPENDIX A

MANUAL TESTING OR NAND/NOR CIRCUIT DEVICES' DC PARAMETERS

APPENDIX A

MANUAL TESTING OF NAND/NOR CIRCUIT DEVICE'S DC PARAMETERS

The probe station used to manually test the DC parameters of the devices in Figure 1(a) and 2 is shown in Figure 49 . The configuration needed to manually test the devices is shown in Figure 48 and photographically in Figure 49. It consists of a curve tracer oscilloscope, the probe station, and camera, television, and interface unit. The process used to determine the parameters manually is shown below:

1. Place wafer onto vacuum chuck with vacuum on.

2. Connect appropriate probe wires from probes to curve tracer. On curve tracer, let C = Drain, B = Gate, E = Source.

3. Select device(s) that appear to be good visually (cracked pads, distorted gate structures, and other obvious distortions were observed in some cases and the devices were not tested).

4. Carefully adjust probes so that they are touching the appropriate pads using Figures 2 and 50 as reference.

5. Use television as an aid.

6. Set curve tracer to appropriate switch selections to provide proper drain and gate voltages and currents.

7. Turn off all lights in room including probe light.

8. Turn curve tracer on and adjust drain voltage until desired I-V curve for the appropriate device appears. If not, remove probes carefully, select another device and repeat the process.

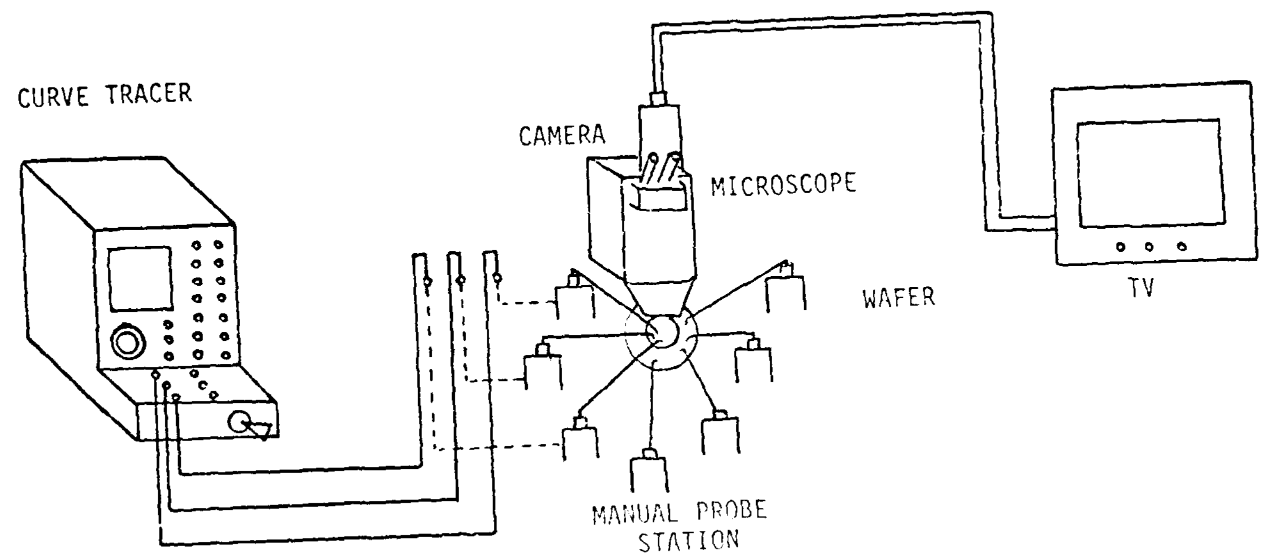

Figure 48. Manual Probe Station Layout.

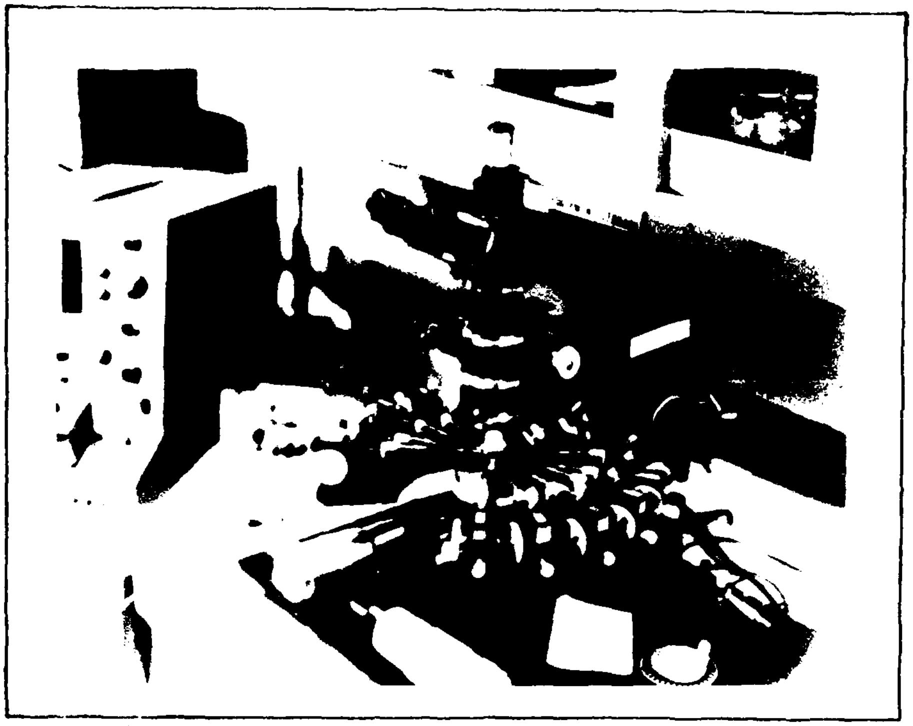

Figure 49. Manual Probe Station and Tektronix Type 576 Curve Tracer.

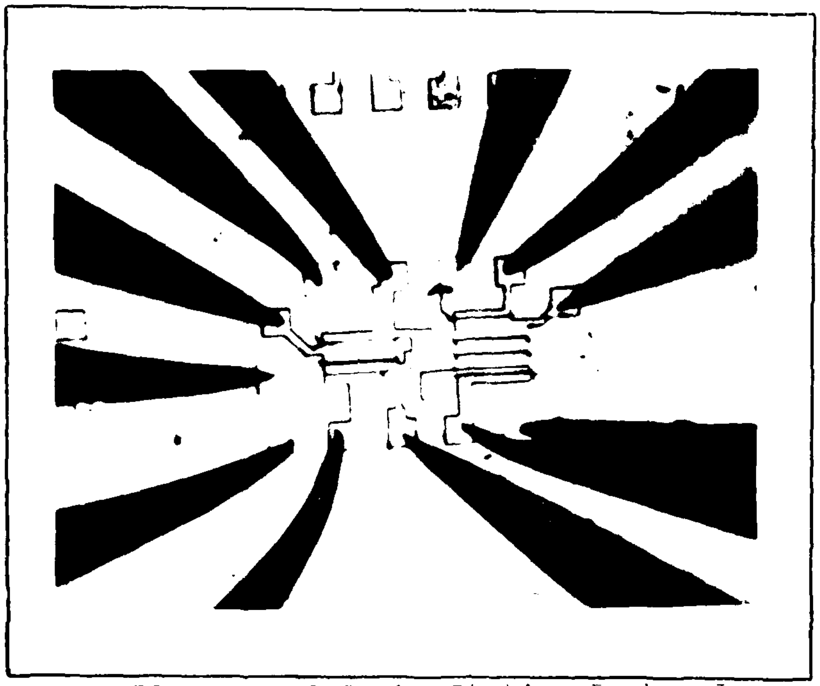

Figure 50. Manual Probe Station Probes In Contact with Pads of GaAs MESFET NAND/NOR Chip.

Manual Testing Results

In this section, the results obtained and problems encountered during the manual testing of the GaAs MESFET logic gate chip (Figure 2) will be presented. Manual testing of the logic gate was necessary for the following reasons:

1. Understand the characteristics of the individual devices of the logic gate.
2. Determine the quality of the individual devices. This would make possible the testing of devices known to be good on the Singer Automated Testing System.
3. Provide data to use for modelling the MESFET.
4. Obtain a spread of the DC parameters.

The DC parameters of each device shown in Figure 1(a) were tested and results obtained in the form of I-V curves. The devices tested were the following:

Source-Follower
Current Source
Active Load
Dual Gate
Single Gate
Schottky Diodes
Test and Probe Resistors

The DC parameters of particular interest for the MESFET's were the following:

I_{DSS}
V_p
R_{on}

g_m

R_{sat}

Breakdown Voltage

The forward and reverse threshold voltages for the three Schottky diodes connected in series as well as the ohmic values of the probe resistor and test resistor were also obtained.

Source Follower. A source-follower's I-V curves are shown in Figure 51. Several source-followers were tested, and it was determined that Figure 51 would depict the best characteristics obtained for a source-follower. It can be observed that excellent linearity in the ohmic and saturation regions was obtained. From the photograph, the curve tracer settings were 500μA/vertical step (I_D), 2V/horizontal step (V_{DS}) and 500mV per step (V_{GS}). The top curve represents V_{GS} = 0. I_{DSS} was obtained at about 3.85 mA. The transconductance, g_m, as shown in the photograph, is 2 mmhos. R_{on} varied from 1500 to 5000. Breakdown voltages were obtained at drain bias voltages of from 8 to 12 V.

Current Source. The current source's I-V curves are shown in Figure 52. From the photograph, it can be observed that the current source tested exhibited linearity in the ohmic region and the saturation region below V_{GS} = -3V. Between V_{GS} = 0 and V_{GS} = -3V, the device seems to be trying to go into breakdown prematurely at about V_{DS} = 4.5. I_{DSS} is found to be about 10 ma at V_{GS} = 0 while V_p is -8V at I_D = 0.1 ma. R_{on} varies from 250 ohm to an extremely high resistance at

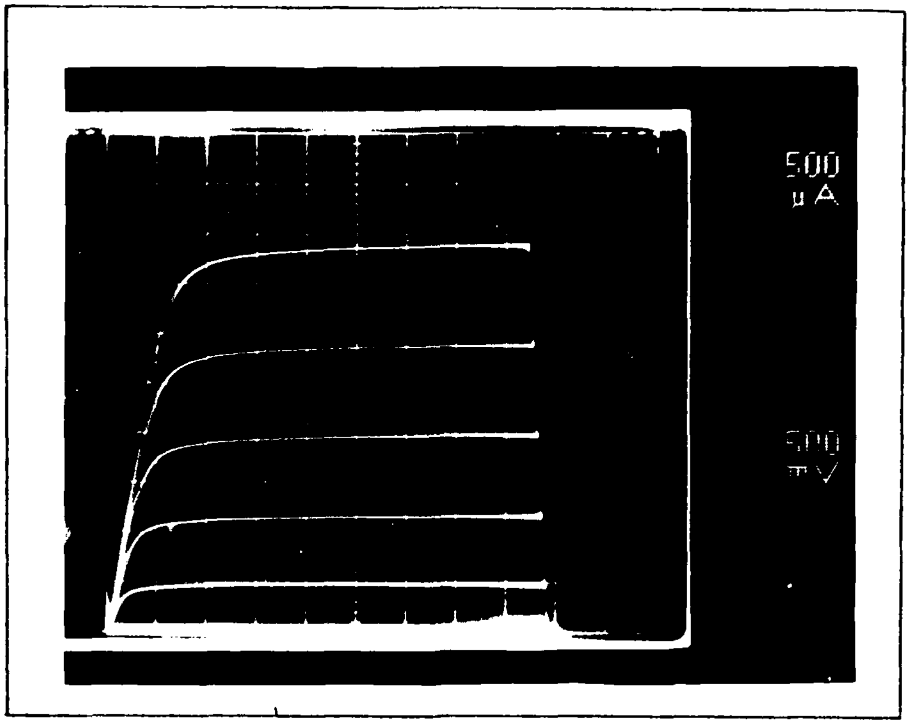

Figure 51. Manually Tested Source Follower Characteristics.

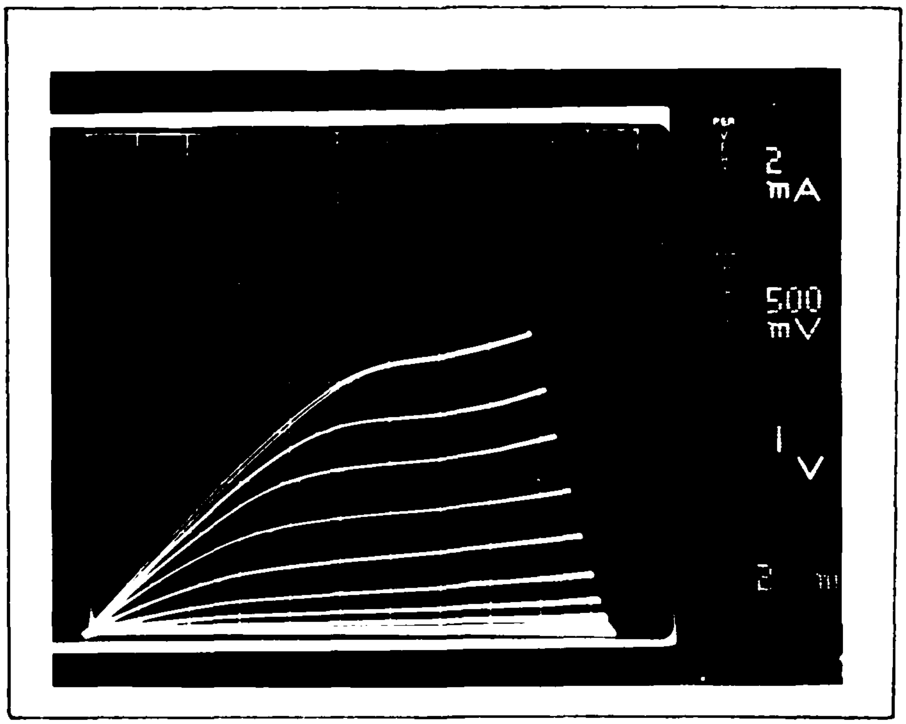

Figure 52. Manually Tested Current Source Characteristics.

pinchoff while R_{sat} varies from 1100 ohm to an extremely high resistance at pinchoff. Transconductance as shown in the photograph is 2 mmhos.

<u>Active Load.</u> An Active Load's I-V curve is shown in Figure 53. With the gate connected to the source, the device exhibits no gain characteristics as can be seen in the photograph. The Active Load, however, exhibits excellant linearity. The device indicates I_{DSS} to be approximately 17.0 mA at V_{DS} = 5.0V. Several Active Loads were tested and the good devices tested indicated similar characteristics as those shown in Figure 53.

<u>Dual and Single Gates.</u> Several dual gates and single gates were tested manually. Prior to testing these devices, the dual gates were observed to determine whether or not the gate structures were damaged. Many of the gates were shorted and therefore would not be able to provide good results. AFWAL/AADE has had problems in fabricating good dual gates. The gate structures were difficult to fabricate due to their extremely small widths of 100 microns, as well as the laboratory's difficulty in apply metallization to the gates to form a Schottky barrier.

The characteristics of a dual gate and single gate of Figure 19 are shown in Figure 54. The gates were tested by applying voltages to the A and C inputs using a curve tracer. (No input voltage was applied to the B input). As shown in the figure, I_{DSS} was obtained at about 27mA. Pinchoff occurred at about -8v at I_D = 0.01mA. Values of R_o varied from 75 to 150 ohms. R_s varied from 200 to 500 ohms. Transconductance for the device is 5 mmhos.

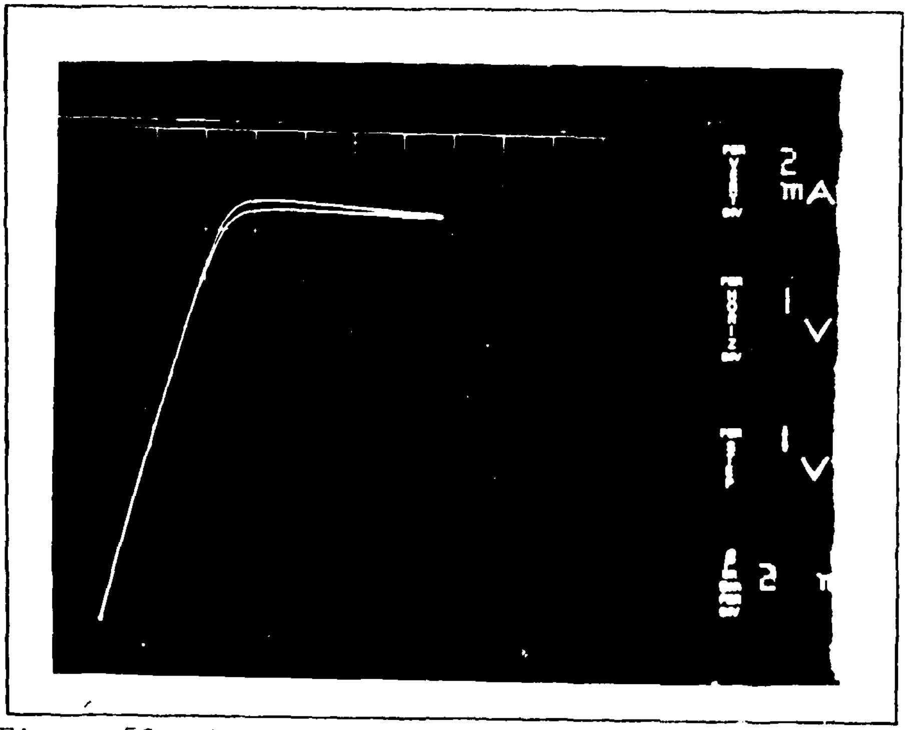

Figure 53. Manually Tested Active Load Characteristics.

Figure 54. Manually Tested Dual and Single Gate I-V Characteristics.

Schottky Diodes. The level shifting Schottky diodes (3) connected in series in Figure 19 were tested and the results are shown in Figures 55 and 56. The forward threshold voltage is about 4V and 0.5 mA according to Figure 55. The reverse threshold voltage is about 8V at 1μA.

Test and Probe Resistor Measurement. The test and probe resistors of Figure 19 were manually tested using the curve tracer. The results are shown in Table X.

Table X. Test and Probe Resistors Measurement Results

RESISTOR	I(A)	V(mV)	RESISTANCE(Kohms)
TEST	50	500	10
	57	500	8.7
	49	500	10.2
PROBE	360	1	2.7
	400	1	2.5

Summary

As a result of testing these devices, a better idea as to how to automate the manual process was obtained. It was realized that automatically testing the single and dual gate devices separately would be difficult due to the fact that either device must be pinched-off before the other can be tested.

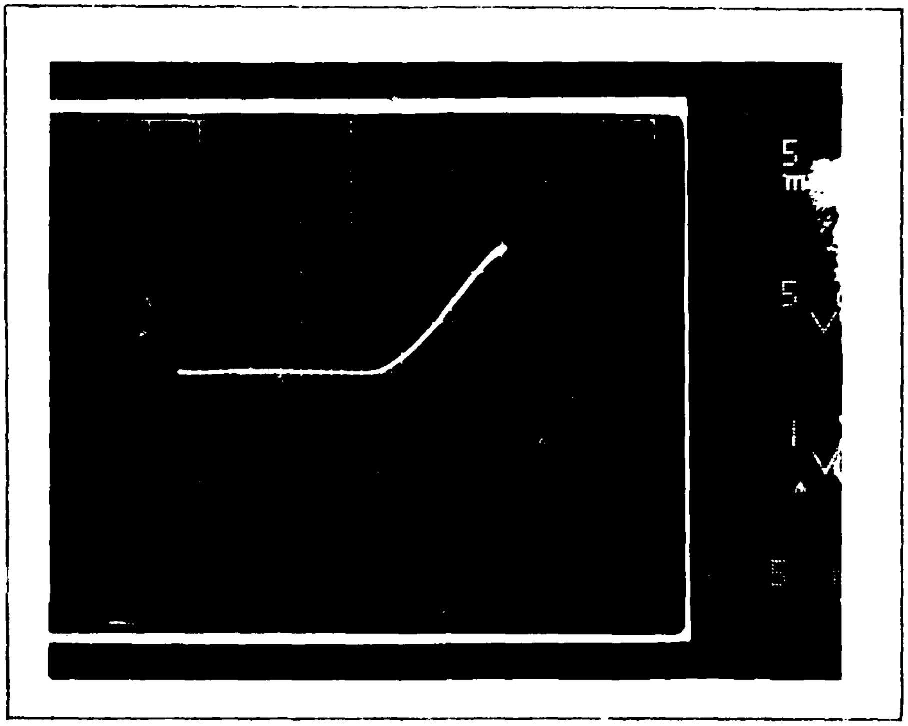

Figure 55. Schottky Diodes' Forward Characteristics.

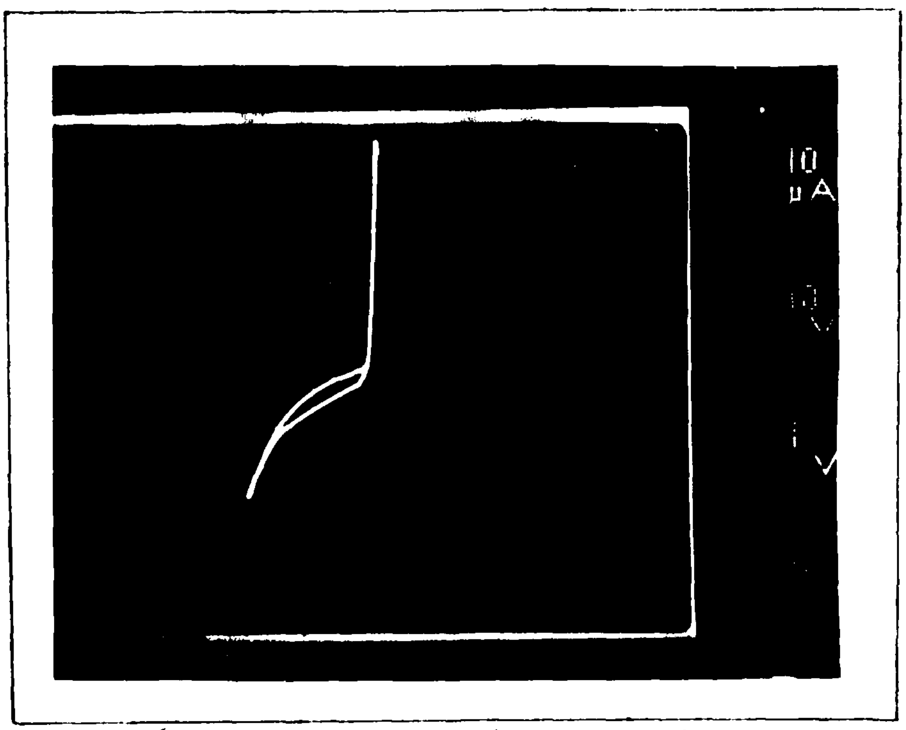

Figure 56. Schottky Diodes' Reverse Characteristics.

APPENDIX B

THE SINGER AUTOMATIC INTEGRATED CIRCUIT TEST SYSTEM

APPENDIX B

THE SINGER AUTOMATIC INTEGRATED CIRCUIT TEST SYSTEM

Description

The Automated Integrated Circuit Test System is capable of performing full DC parametric testing, data logging, data plotting, and data analysis on itnegrated circuits (Ref 21). The system may be used to test circuits at the wafer level using a TAC (Transistor Automation Corporation) Automated Probe Unit (Figure 65). Discrete components can be tested on the system as well.

The primary function of the system is to test the DC parameters of a device or devices. DC parametric testing is defined as measuring IC voltages, currents, and values of IC resistors at high accuracy and at low stimulus test frequencies under program control.

A Varian Omnitask Minicomputer utilizing 32K core of memory controls voltage and current source supplies, necessary peripherals, a digital voltmeter, and the TAC probe mentioned above. In addition, via an instrument control board, the Varian selects the individual supplies and voltmeter using a complex matrix system as shown in Figure 57.

A block diagram of the entire system is shown in Figure 58. A photograph and drawing of the Singer system are shown in Figures 59 and 60.

Test System Subsystems

The Singer test system consists of several subsystems which together provide the capability of forcing voltages and

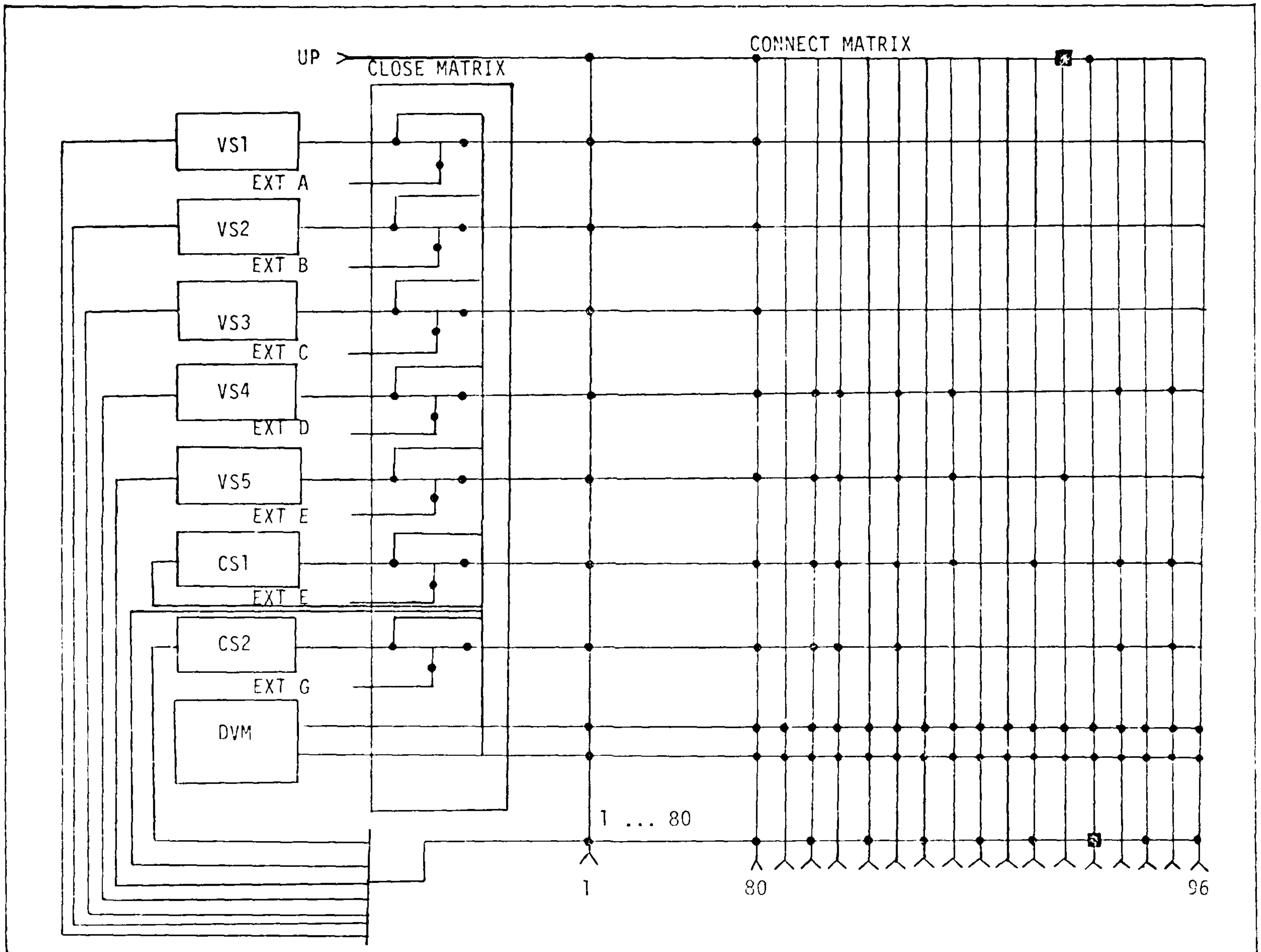

Figure 57. Singer Tester Measurement System Block Diagram.

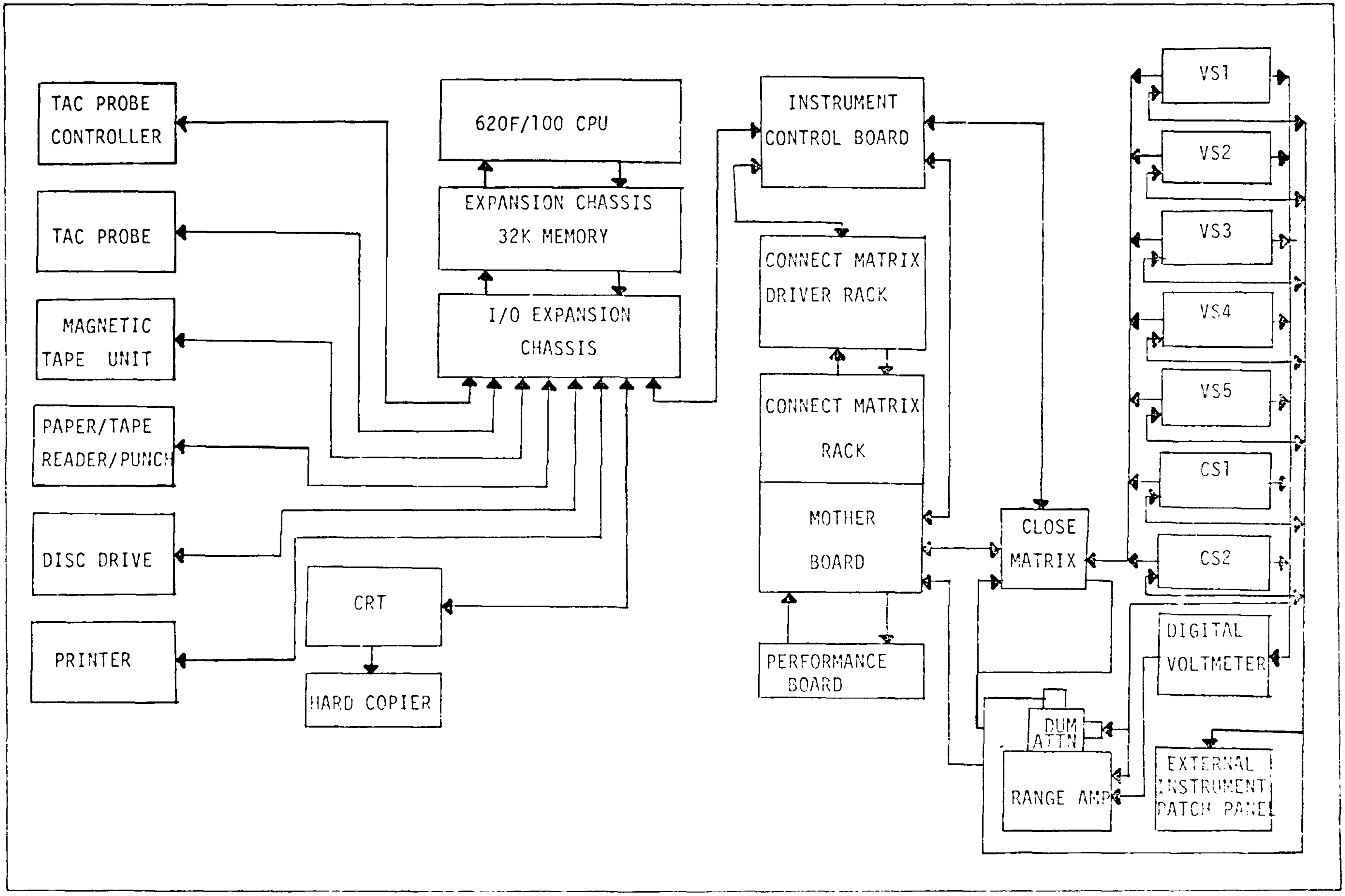

Figure 58. Singer Tester System Block Diagram.

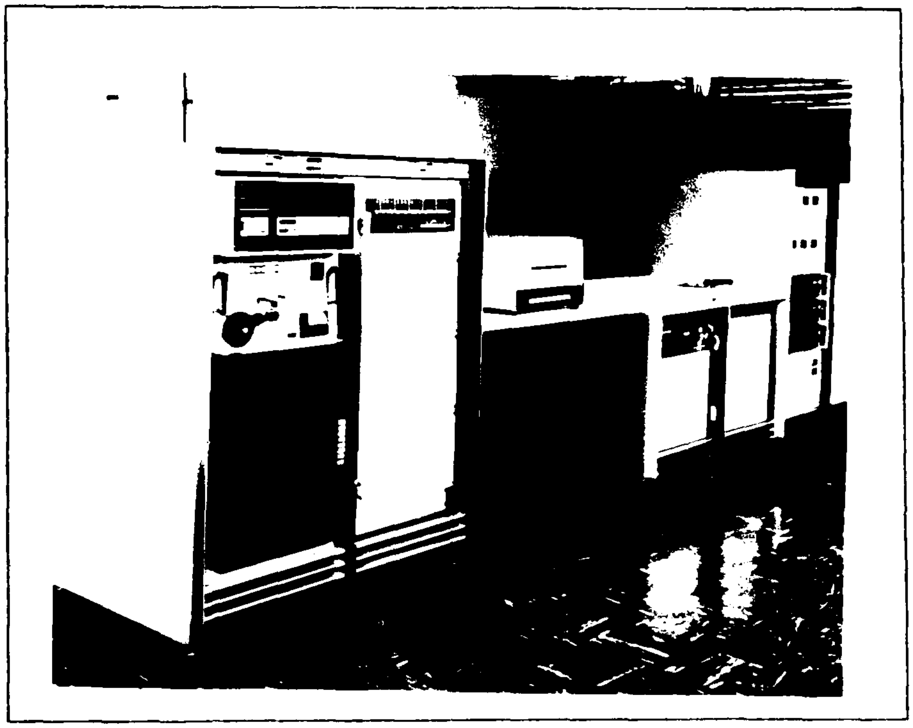

Figure 59. The Singer Automatic Integrated Circuit Test System.

currents, as well as conducting DC parameter measurements (voltage, current, and resistance). In addition, a DC switching subsystem is included. This system provides the connection of any of the voltage or current sources, common instrumentation ground, or user matrix input, to any one (or more) of the 80 test fixture pins under test program control provided by the Varian.

DC Voltage Measurement Subsystem. The DC Voltage Measurement subsystem has the capability to measure, under test program control, DC voltages between any two of the 92 test pins (80 measurement/forcing, 15 measurement only pins, 1 user matrix input pin, and 1 common instrumentation ground pin).

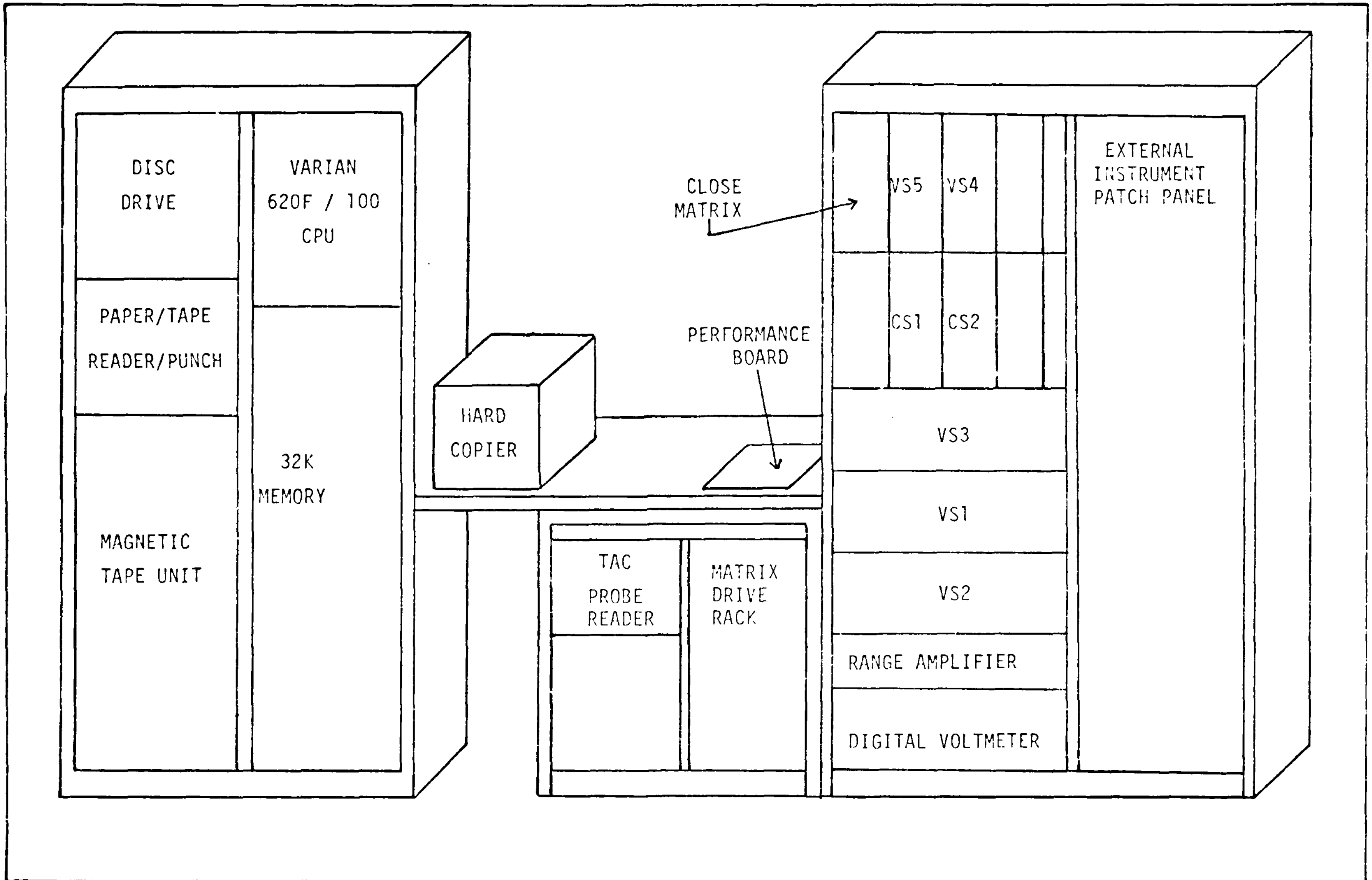

Figure 60. Physical Layout of the Singer Automatic Integrated Circuit Test System

The DC voltage measurement capability is as follows:

A. Ranges: $\pm$ 100mV full scale to $\pm$ 200V full scale

B. Resolution: $\pm$ 0.001% of range

C. Accuracy: $\pm$ 0.01% of the absolute DC voltage present at the test pin.

D. Input Impedance: at least 10 megohms on all ranges

DC Current Measurement Subsystems. The DC Current Measurement subsystem has the capability to measure, under test program control, DC currents drawn by a device (transistor, resistor, diode) connected between any two of the test pins of the matrix.

The DC current measurement capability is as follows:

A. Range: 0 to 1.0 ampere.

B. Current Measurement Accuracy: $\pm$ 1% of actual value.

C. Current Limit Range: 0 to 1.1 amp.

D. Current Limit Resolution: $\frac{I_{RANGE}}{2} \times 10^{-3}$ amps.

DC Resistance Measurement Subsystem. The DC Resistance Measurement Subsystem has the capability to measure, under test program control, the DC resistance of an integrated circuit or discrete resistor connected between any two pins of the matrix.

The DC Resistance measurement capability is as follows:

A. Ranges: 10.0 ohms full scale to 200k ohms full scale.

B. Resolution: $\pm$ 0.001% of the range

C. Accuracy: $\pm$ 0.04% of the absolute resistance between the two test pins being measured.

The subsystem uses Kelvin wiring and switching techniques in order to provide accurate and repeatable resistance measurements. In addition, the subsystem uses a 4 terminal type of measurement which consists of two DC voltage sense lines and two ohms "signal" lines.

The subsystem is thus configured by using one of two constant current programmable power supplies contained in the test system as the ohms "signal" lines, measuring the voltage across the resistor under test with the DC voltage measurement subsystem and using the System controller to calculate the resistance in ohms.

DC Stimulus Subsystem. The DC stimulus subsystem provides five programmable voltage sources (VS1-VS5) and two programmable constant current sources (CS1 and CS2) as shown in Figures 57 and 58. Each source is independently programmable in various modes of operation which will be described in the following paragraphs. Each source has internal over-voltage and over-current protection and makes use of a floating Kelvin type of output which consists of analog high, analog laws, sense high, and sense low.

Each source reduces digital noise on the analog output using isolated control logic. Additionally, each source contains its own internal memory which acts as a storage buffer for programming data. The output of each source remains constant until a change is initiated by the Test System Controller.

The programmable power supplies, VS1, VS2, and VS3 have the following spedifications:

A. Output Voltage: 0 to ± 16.0V in 1.0mV increments

B. Output Current: 0 to ± 100mA, Short-circuit protected

C. Current sink capability: ± 50mA, overload protected

D. Accuracy: 0.01% of the programmed value (which depends on the condition of the power supplies due to calibration inaccuracies or component failure in the sources themselves.

E. Load regulation: 0.001%

F. Line regulation: 0.001% for a ± 10% change in line voltage.

The programmable voltage power supply, VS4, is a voltage forcing-current measuring DC source with the following specifications:

A. Output voltage ranges: 0 to ± 32.0V full range:
0 to ± 9.0V in 1.0mV increments:
And ± 8.0 to 32.0V in 4.0mV increments.

B. Output voltage accuracy of programmed value:
± 0.5% of the full scale voltage range.

C. Output Current range: 0 to ± 100mA minimum.

D. Current measurement ranges and resolution requirements:

FULL SCALE MEASUREMENT RANGES	RESOLUTION
0 to ± 4.0μA	± 1nA
0 to ∓ 32.0μA	∓ 10nA
0 to ∓ 250μA	∓ 100nA
0 to ∓ 2.0mA	∓ 1μA
0 to ∓ 16.0mA	∓ 10μA
0 to ∓ 100.0mA	∓ 100μA

E. Current measurement accuracy: ± 1.0% of the actual value.

F. Current limit: ± 110.0% of the full scale current measurement range.

VS5 is a programmable voltage power supply and it functions as a voltage forcing-current measuring unit with the following designed specification:

A. Output voltage ranges: 0 to ± 16.0V full range; 0 to ± 9.0 volts in 1.0mV increments; and ± 8.0 to ± 16.0 volts in 4.0 mV increments.

B. Output voltage accuracy of programmed value: ± 0.2% of full scale voltage range.

C. Output current range: 0 to ± 1.0 Ampere, minimum.

D. Current measurement capability: 0 to ± 1.0 Ampere.

E. Current measurement accuracy: ± 1.0% of the actual value.

F. Current limit: ± 110% of the full scale current measurement range.

CS1 is a programmable constant current source and functions as a current forcing-voltage measuring unit with the following specifications:

A. Constant current output (Programmable):

FULL SCALE RANGES	RESOLUTION
0 to ± 500nA	± 100 pA
0 to ± 5μA	± 1 nA
0 to ± 32μA	± 5 nA
0 to ± 250μA	± 50 nA
0 to ±2 mA	± 1μA
0 to ± 16mA	± 3μA
0 to ± 100mA	± 20μA

B. Programmed accuracy of the programmed constant current value: ± 1% of the programmed value.

C. Voltage measurement accuracy: ± 2.0% of the actual value, from 0 to ± 32.0 volts DC.

D. Voltage output range: 0 to ± 35 volts minimum (110% of the full scale voltage measurement range) with a programmable clamp voltage of 1.0V increments minimum.

CS2 is a programmable constant current source that functions as a current forcing-voltage measuring unit with the following specifications:

A. Constant current output (programmable):

FULL SCALE RANGES	RESOLUTION
0 to ± 250μA	± 40 nA
0 to ± 2 mA	± 250 nA
0 to ± 15 mA	± 2 μA
0 to ± 100 mA	± 15 μA

B. Programmed accuracy of the programmed constant current value: ± 1% of the programmed value.

C. Voltage measurement accuracy: ± 0.2% of the actual value from 0 to ± 100 volts DC.

D. Voltage output range: 0 to ± 110 volts, minimum (110% of the full scale voltage measurement range) with a programmable clamp of 1.0V increments minimum.

System Test Fixture/Performance Board

The System Test Fixture/Performance Board is defined as the unit which interfaces a device (integrated circuit (MSI) elements such as transistors, resistors, and diodes, discrete transistors and resistors and discrete diodes) under test and its associated "performance circuits," to all measurement and stimulus subsystems contained in the test system. A performance circuit is defined, according to the reference used, on a per pin basis, as a

> "Special circuit, such as a passive load, an active load, a capacitive load, or a special interface circuit, which is connected to some pins of the device to allow stimulation of realistic device operation conditions during the test procedure." (Ref 21).

DC Switching Subsystem

An 11 x 80 (Kelvin (2 wire) high reliability shielded mercury wetted and dry reed relay matrix is provided which allows the Kelvin connection of any of the sources (VS1 through VS5, CS1 and CS2), the common instrumentation ground, or the one user matrix input, to any (or more) of the 80 test fixture pins under test program control (Refer to Figure 57).

Each reed relay pair (Kelvin matrix crosspoint) in the matrix has independent storage capability. Independent storage is the ability to remain in one of two switched states (after initial programmed switching by the test system controller) without the need for further holding commands from the test system controller. A master matrix clear line is provided that will disconnect all inputs to the 80 pins of the test fixture under program control.

All cabling connections are made of high quality shielded cable with shield grounding techniques used so that system ground-loops are minimized.

A shielded, 92 input (minimum) 2 wire reed relay matrix is provided which allows the two inputs (high and low) of the DC Voltage Measurement Unit to be switched under test program control, to any two of the 92 test pins.

Close Relay Matrix/External Instrument Multiplexer

A special relay network is provided so that any one of the instrumetns (VS1-VS5 or CS1 and CS2) can be replaced by an external instrument under program control as shown in Figure 57. The matrix is designed so that either, but not both, VS1 or External A device may be closed to the main switching matrix which applies to all instruments except for the DVM bus. The external devices can be alternate power supplies that remain at a voltage or current value determined by the programmer and are not programmed by the programming language. The Close Relay Matrix and associated matrix sections will be discussed further in Appendix D.

Instrument Control System

The Varian Computer transmits signals to the buffered I/O controller located in the I/O Expansion Chassis which are in turn sent to the Instrument Control rack to control the entire system. The Instrument Control rack contains receivers, decoders, and timing circuits to control the 7 power supply instruments, close relay matrix box, 16 external relay drivers available at the relay motherboard, and the analog-to-digital (A/D) converter including the ranging control on the A/D input amplifier.

Test System Controller

The user programmed Test System Controller controls all programmable elements contained in the test system with the following characteristics:

A. Memory capacity: supplied with 32K works within the mainframe.

B. Memory cycle time: 1 μsec or less.

C. Word length: 16 bits.

D. Memory addressing: direct.

E. Supplied with a ROM bootstrap loader.

F. Input/Output channels: Two input/output channels are provided to allow for user installed test instrumentation to interface to the test system controller. Each I/O channel has the capability to input 16 bits and output 16 bits under test program control via plug-in interface cards. This enables the ability expand the the capability and reconfiguration of the test system.

G. Controller memory has the ability to retain stored information for one week without test system power.

H. A Direct Memory Access Channel (DMAC) is used with the dual magnetic disc unit.

I. Necessary time delays required for proper operation of all test system instrumentation can be generated under test program control.

The Test System Controller consists of the VARIAN 620/f-100 minicomputer, 32K memory expansion unit, and an I/O expansion chassis.

System Controller Peripherals

The System Controller peripherals are shown in Figure on the far left side.

Keyboard Entry and Information Printout Unit. A Texas Instruments Silent 700 table-top high speed teleprinter is used to input programs required for real-time testing. The teleprinter has the capability to transmit and receive data from the test system controller at speeds up to 300 words per minute or 30 cps. The unit is sued as the main I/O unit for the controller.

High Speed Paper Tape Reader/Punch Combination. The test system is supplied with an optical 300 cps paper tpae reader/ punch combination with the capability to operate in the step or continuous mode. The reader uses an 8-level code while the punch is capable of punching 75 characters per second and has the ability to duplicate the tape being read by the reader.

Magnetic Disc Unit. The test system uses a moving head dual magnetic disc driver unit (PERTEC 3000) which uses two upper and lower disc cartridges. The lower disk is permanently installed with the disk driver unit itself and is used to store the operating system software for the computer. The upper disk is a removable hard pack used to store all user programs. The total storage capability is at least 2 million 16 bit words.

Information Display Terminal. A Tektronix Model 4012-1 Display Terminal (hard copy compatible) is supplied with the test system. The unit allows input and output of alphanumeric data and the output of graphic data at an input/output data rate of 9600 bits/sec. The display terminal use is that of scheduling DC parameter test runs, calibration runs, the assignment of logical unit names to the peripehrals, and providing the user (or programmer) the ability to communicate with the operating system.

Information Display Terminal Hard Copy Unit. A Tektronix Model 4610 hard copy unit is connected to the display terminal. The hard copy unit produces permanent high-resolution, dry copies from the display terminal.

Magnetic Tape Unit. A WANGCO Model 10, 7 track magnetic tape unit, is supplied with the system. The tape unit it IBM compatible and has a data density of 556 (HI)/200(LO CPI).

Line Printer. The Data Products Model 2410 Line Printer (not shown in Figure 58), but connected to the I/O Expansion Chassis) is sued to output source programs as well as data. Speeds ranging rrom 245 lines per minute, and 132 columns, to 1110 lines per minute, and 24 columns of printed characters from a 64-character set are possible.

TAC Probe and Controller. The TAC Probe and Controller are discussed in Appendices C and G.

APPENDIX C

TEST SYSTEM SOFTWARE

APPENDIX C

TEST SYSTEM SOFTWARE

Test System Software Package

The test system is furnished with a software package to permit the user or programmer to write test programs. The system monitor program controls the overall software operation of the test system which initiates all input, output, data analysis, and control of the test system during system operation (Ref 21). A simple, English-like test oriented language called Elucidate, is the programming language for the system and will be described later in this Appendix.

Compiler. On-line program translation is supplied with the test system by the software package. A disc resident compiler configured to match the system hardware comprises the software package. The compiler operates in the batch processing mode in conjunction with the Source Editor for corrections. A start execution, RUN, executes the test program after it has been compiled and all diagnostic errors removed.

Editor. In addition, on on-line test program editing capability is provided. The on-line test program editor allows the programmer to change or add instructions or test sequences, and delete instructions or test sequences via the teleprinter keyboard.

VORTEX Operating System. An on-line magnetic disc operating system is also included in the software package. The disc operating system, known as VORTEX (Varian Omnitask Real-Time Executive) is capable of:

A. Loading the configured test system software into core memory from the disc.

B. Storing test programs written in the Elucidate test language onto the disc.

C. Loading test programs from the disc into core under operator and test program control.

D. Executing test programs under operator control.

E. Deleting test programs on disc.

F. Repacking the disc.

G. Storing and recovering test data under control of a test program.

H. Linking test programs in order for a new program to be loaded from the disc under control of a resident test program and automatically executed. This new program replaces the requesting program in core.

I. Storing, recovering, and executing machine object code resulting from compilation of FORTRAN and assembly language programs.

J. Storing, recovering, and executing utility programs.

Available Programming Languages. In addition to the Elucidate test language, FORTRAN IV and assembly languages are supplied to allow for user data processing. The user is also capable to write assembly language programs for any additionally installed instrumentation.

Software Drivers. Software drivers are supplied for all test system instrumentation, including Automation Corporation Automatic probe unit. The software driver for the TAC probe controller enables a test program to completely control the

TAC probe unit (See Figure 65, Appendix G). The following items are controlled by the software driver under test program control:

A. Sense the up or down position of the z-stage.

B. Move the z-stage to the up or down position.

C. Control the in-place inker on the probe unit.

D. Initiate an independent or simulataneous X and Y indix operation.

E. Control independently the X and Y step size.

F. Sense the completion of an index operation.

G. Sense the Start Test signal from the probe controller.

H. Sense the Emergency Stop signal line from the probe controller and create a priority interrupt to the test system controller if an Emergency Stop condition occurs.

Graphics. The Advanced Plot-10 Tektronix software package is supplied with the display terminal to provide a graphics capability for the system.

Elucidate Programming Test Language Description

The Varian 620/f-100 computer controls a real-time test situation and requires certain specialized logic elements (Ref 22). The Elucidate programming language combined with the logic elements of the Singer test system provides the computer with an error free test device. A 16-bit binary data word transferred from the computer to the test system (power supplies, digital voltmeter, etc) is the basic element of the Elucidate control system. The test system uses a three dimensional array concept of X, Y, and Z addressing. This allows the Elucidate programming language to define the necessary control functions to the test system. To accomplish this, the 16-bit binary word is divided into four elements. The first element is a 1-bit word which separates test system commands and computer control words. Element two is a 5-bit "VERB" field used to define an action which the test system must perform. A typical verb is "SET" which is used in an instruction such as

SET VS1 4.5V, 10.0MA

where "SET" sets the voltage output of power supply VS1 at 4.5V and at a maximum limit or clamp current of 10.0MA. A maximum of 31 verbs is provided by the Elucidate language. The third element is a 5-bit "NOUN" field which is defined as the place where an action occurs. A typical noun in "VS1" as in the above command. The fourth element is the "MODIFIER" which consists of 5-bits which are used to describe the test point locations. A modifier can be an integer or real number, unit of measure, or a variable. In the case of the above command, 4.5 and 10.0 are real numbers, whereas V(volts) and MA(milliamps) are units of measure. One 16-bit word is not adequate to describe the required conditions for certain actions which the test set performs. A multiple word command is used in this case with the first word containing VERB, NOUN, and MODIFIER, and the following words specifying additional conditions in a predetermined format. The above command is such an example. The modifier "10. [illegible]" is an additional condition specifying that a circuit installed in the test system can draw a maximum current of about 10.0mA from VS1.

The three-dimensional address location can describe any function required of the test system. Each function, therefore, normally has a three input gate that consists of a VERB, NOUN, and MODIFIER. With all three inputs true, that function and only that function will activate. The Elucidate language easily has control of this complex system using this addressing scheme.

The Elucidate Compiler transforms English commands and numeric locations to the 16-bit data words comprehensible by the test system. The compiler is written in DAS MR MACRO assembly language with access to the compiler gained through the Test Set Operating System (TSOS) which is then accessed by the Varian's VORTEX operating system.

From the previous discussion, Elucidate is a unique test language. It is a simple language, but it is necessary to describe it further to understand the MESFET program.

After the items in the previous section were determined, the power supplies were required to be initialized using the following commands as an example:

```
100     :CONDITION TEST SYSTEM FOR TESTING
110      RESET
120      ENABLE VS1: VS2;VS5
130      CLOSE GND;  VS1;VS2;VS5
140      CON GND 40; VS1 41; VS2 36; VS5 48
```

The RESET command initialized the matrix system (removed power supplies, voltmeter, et cetera from the matrix). In other words, it caused the test system to be reset to a neutral condition with all previous commands negated. After every RESET, the remaining commands were required. The ENABLE command signalled the power supplies to switch to the on state. The CLOSE command provided the capability to pre-establish the power supplies and ground (GND) selected prior to the connection of the test point matrix pins. The CON (CONNECT) command connected the power supplies and GND to the individual test point matrix pins. A DIS (DISCONNECT) negates the CON command. From this point on, the power supplies had to be set at the desired voltage and current clamp value using the following command:

150   SET VS5 5.0V, 20.0MA

The SET command sets VS5 to 5.0V at the maximum allowable clamps current drawn by a device at 20.0MA. To measure this voltage, the voltmeter must be connected using

160   CON VMH 48; VML 40

The CON command connects the voltmeter between pins 48 and 40. VS5 is also connected at pin 48 and GND at 40. Therefore, when the command

170   READ VMH 4

is reached, the voltmeter is read at approximately 5.0V ($\pm$ 0.01% of the absolute DC voltage present at the test pin). The above command not only caused a measurement to be taken, but stored the measurement with the line number as a reference location for the data obtained. In addition, the integer 4 or MOD number was specified with 2^4 or 16 measurements actually taken and averaged. A print command using the line number location of the measurement caused the voltage measurement obtained to be printed with the unit V or volts.

Current measurements were made using the following command:

180   READ VS5 4

Current was measured and averaged as before with a print command (not shown) printing the current in A or amperes. Appropriate conversion to MA was obtained by multiplying the results at line 180 by 1000.0 and substituting MA for A using formatting.

Call to subroutines are made using the following command:

190 GOSUB 1330: CALL PINCH-OFF VOLTAGE (UP) SUBROUTINE

The subroutine was called to an ENTER statement located at line 1330. A GOTO statement placed before entering the subroutine was then necessary to prevent accidental entry to the subroutine (not shown). The GOTO statement, when reached, skips the entire subroutine and continues with the next statement. A RETURN command returned control to the main program. All results obtained in the subroutine were automatically carried to the main program and remained the same until the subroutine was entered again.

Variables were used throughout the program using only Elucidate variables, ZA, ZB,...ZZ. Measurements taken were set equal to variables using the command,

200 EQ, ZA, 180

where ZA was set equal to the measurements taken at line 180. To set a variable to an integer or real number, the command

210 EQ, ZA, 250.0

had to be used to distinguish the difference between a line number and, an integer or real number.

Simple algebraic manipulations could also be performed (multiply, add, divide, subtract). These commands and their variations are shown below as an example:

```
220    MUL,170,1.0
230    DIV,170,180
240    SUB,170,ZA
250    EQ,ZB,7.0
260    ADD,170,ZB
```

At line 220, using the previous commands presented at their respective line numbers, the voltage reading is multiplied by 1.0 and the result stored at line 170. At line 230, line 170 is divided by the current reading at line 180 with the result stored at line 150. Afterward, line 170 is subtracted by ZA = 250.0 with the result stored at line 170. The variable ZB is set equal to 7.0 and then added to the result at line 170 with the final result stored at line 170.

APPENDIX D

MATRIX CONTROL OF THE TEST SYSTEM

APPENDIX D

MATRIX CONTROL OF THE TEST SYSTEM

Figure 57 of Appendix B is a basic diagram of the Elucidate controlled system (Ref 22). The output of the test system at any test point is subject to a selection of switches. The instruments or power supplies are connected to the voltmeter via the proper switch. These switches or relays are controlled by the compiler which allows only those commands that are technically feasible. Other checks are made to safeguard the hardware.

Five test equipment (matrix) control verbs are provided: CLOSE, OPEN, CONNECT, DISCONNECT, and RESET. CLOSE provides the capability to pre-establish the instrument selected prior to connecting the test point matrix to the instrument. The OPEN command negates the CLOSE command.

The verb CONNECT and its negative, DISCONNECT, are used to connect/disconnect individual test points to various instruments.

The verb RESET returns all relays to their DISCONNECTED, OPEN state and does not have nouns associated with it.

In order to prevent undesirable combinations of switching, the following rules presented in the programming manual (Ref 22) were established for the system:

A. All nouns (or instruments) except the voltmeter (VMH, VML) and resistance measurement instrument (RMH, RML), must be CLOSED before being CONNECTED.

B. The voltage and current supply nouns (VS1-VS5, CS1 and CS2) may not be closed with their respective externals.

For example, VS1 may not be closed with External A instrument at any matrix switching connection or pin.

C. Each noun is classified as a forcing type of sensing (measuring) type.

D. Forcing nouns (power supplies) can be connected to as many pins (testpoints) as desired; however, no two forcing nouns may be connected to one pin at the same time.

E. Sensing nouns (voltmeter) can be connected to only one pin at a time; however, there is no restriction as to cross connection of these nouns.

F. Since the voltmeter is differential (described by two nouns, Voltmeter Measure High (VMH) and Voltmeter Measure Low (VML), both VMH and VML must be connected before the voltmeter is read. This holds true for Resistance Measure High and Low (RMH and RML).

Table XI shows the interrelation of Elucidate verbs and nouns by indicating their allowable and required combinations.

TABLE XI

VERB/NOUN APPLICABILITY TABLE--MATRIX CONTROL VERBS

	VERBS						
NOUNS	CLOSE	OPEN	CONNECT	DISCONNECT	RESET	READ	SET
VS1	X	X	X	X			X
VS2	X	X	X	X			X
VS3	X	X	X				X
VS4	X	X	X	X		X	X
CS1	X	X	X	X		X	X
CS2	X	X	X	X		X	X
EXT A	X	X	X	X			
EXT B	X	X	X	X			
EXT C	X	X	X	X			
EXT D	X	X	X	X			
EXT E	X	X	X	X			
EXT F	X	X	X	X			
UP	X	X	X	X		X	
VMH			X	X		X	
VML			X	X		X	
RMH	X	X	X	X		X	
RML	X	X	X	X			
RELAY	X	X					
GND	X	X	X	X			

APPENDIX E

VARIAN 620/f-100 COMPUTER CHARACTERISTICS

APPENDIX E

VARIAN 620/f-100 COMPUTER CHARACTERISTICS

Varian 620/6-100 Features

The Varian 620/f-100 computer (Ref 23) is a high-speed, general purpose, digital computer for scientific and industrial applications is shown in Figure 61 and has the following features:

Memory cycle time: 750 nsec.

Instruction set size: 142 plus 8 optional instructions.

Word length: 16 bits.

Modular core memory: Expandable to 32,768 words in 4.096 or 8,192-word increments.

Automatic data transfer: Direct memory access (DMA) with transfer data rates to 275,000 words per second; priority memory access (PMA) for transfer rates to 1.3 million words per second.

I/O capability: 64 devices can be placed on the I/O bus with the I/O system expandable to include automatic block transfer, multi-level priority interrupt, and cycle-stealing transfers.

Software capability: DAS 4A,DAS8A, and DAS MR (MACRO) assemblers; binary load/dump (BLD II): debugging (AID II); computer diagnostics (MAINTAIN II); mathematical subroutines; real-time monitor (RTM), source program editor (EDIT); master operating system (MOS) for fixed-and moving-head discs, drum, and magnetic tape; ANSI FORTRAN IV, conversational BASIC; report generator, RPG IV: and an extensive library of programs in the Voice user's group.

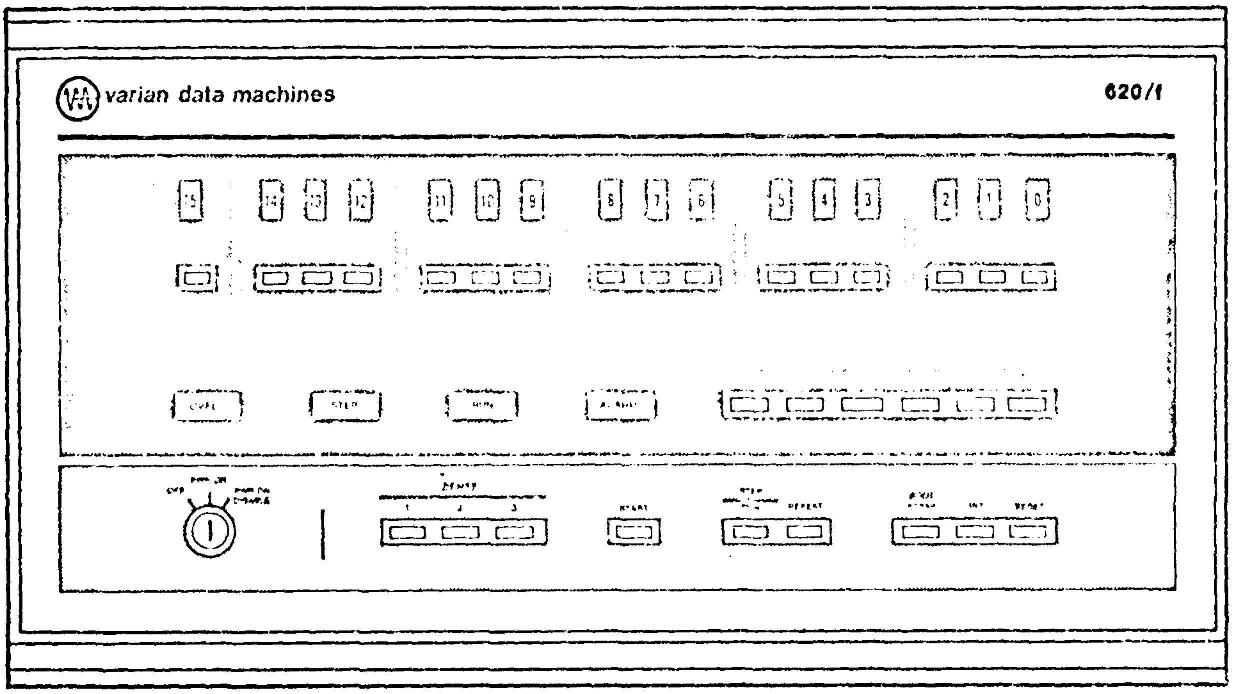

Figure 61. The Varian 620/f-100 Computer.

In addition to the software capability, the Varian compiles Elucidate source code and then converts it into machine language object code using the DAS MR (MACRO) assembler.

Functional Organization. The Varian 620/f-100 computer functional organization is shown in Figure 62. Further information concerning the detailed operation and organization of the 620/f-100 computer is beyond the scope of this thesis. Therefore, the reader is referred to Reference 23.

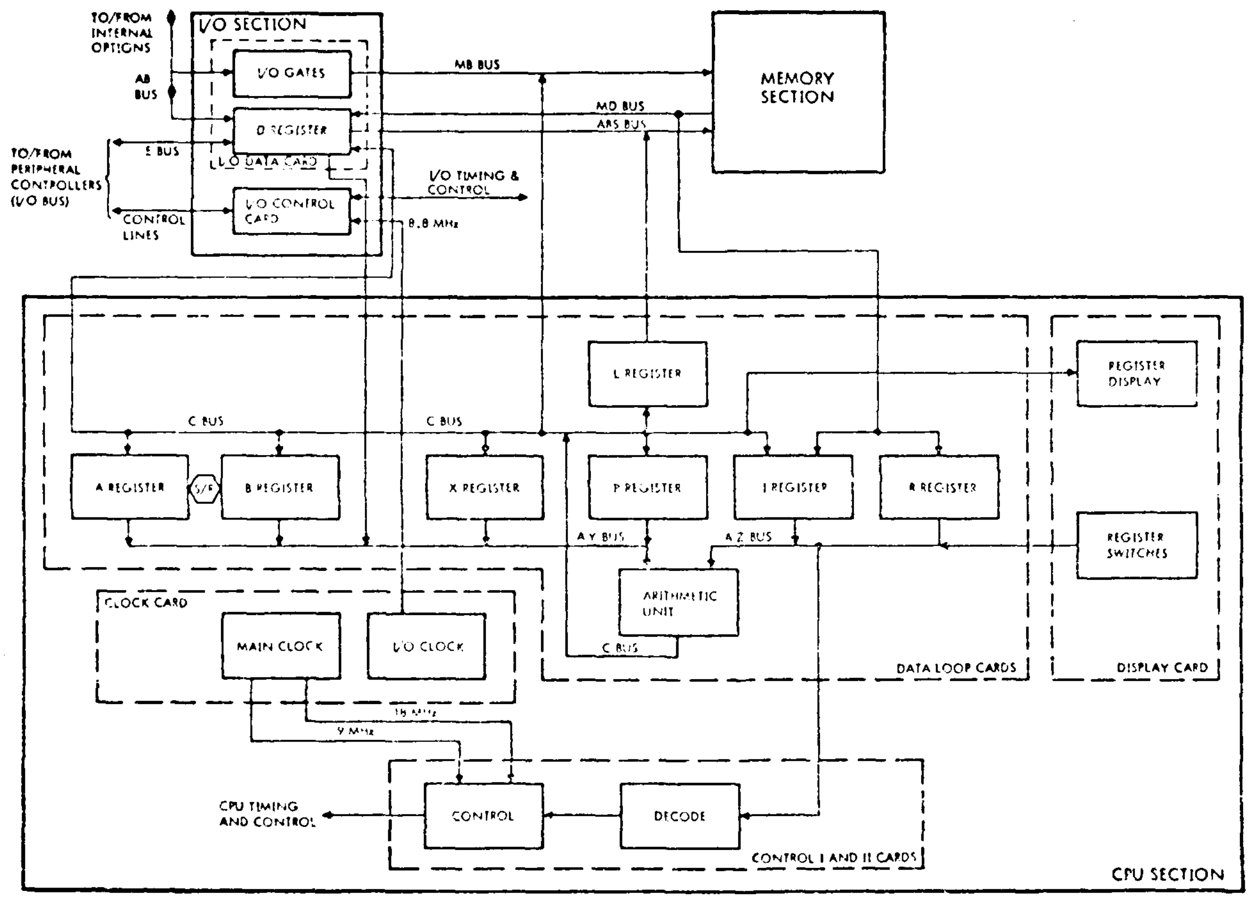

Figure 62. Functional Organization of the Varian 620/f-100 Computer.

AD-A100 762 AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOO--ETC FLD 2
THE AUTOMATED DC PARAMETER TESTING OF GAAS MESFETS USING THE SI--ETC(U)
SEP 80 T L HARPER
UNCLASSIFIED AFIT/EE/GE/80-7 NL

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APPENDIX F

VORTEX OPERATING SYSTEM

APPENDIX F

VORTEX OPERATING SYSTEM

The Varian Omnitask Real-Time Executive (VORTEX) (Ref 24) is a modular software operation system for controlling, scheduling, and monitoring tasks in a real-time multiprogramming environment. VORTEX provides for background operations such as compilation, assembly, debugging, or execution of tasks not associated with the real-time functions of the system.
VORTEX is comprised of the following basic features:

- -Real-time I/O processing
- -Provision for directly connected interrupts
- -Interrupt processing
- -Multiprogramming of real-time and background
- -Priority task scheduling tasks
- -Load and go (Automatic)
- -Centralized and device-independent I/O system using logical unit and file names
- -Operator communications
- -Background programming aids:
  FORTRAN and RPG IV compilers, DAS MR assembler, load-module generator, library updating, debugging, and source editor
- -Use of background area when required by foreground tasks
- -Disk/drum directories and references
- -System generator

System Flow and Organization

VORTEX executes foreground and background tasks scheduled by operator requests, interrupts, or other tasks. All tasks are scheduled, activated, and executed by the real-time executive component on a priority basis. In the VORTEX operating system, each task has a level of priority that determines what will be executed first when two or more tasks come up for execution simultaneously.

The job-control processor component of the VORTEX system manages requests for the scheduling of background tasks. Upon completion of a task, control returns to the real-time executive. For a background task, the real-time executive schedules the job-control processor to determine if there are any further background tasks for execution. During execution, any foreground task can use any real-time executive service.

Important foreground and background tasks are defined below:

Foreground Tasks:

Real-Time Executive (RTE): Processes, upon request by task operations that the task itself cannot perform.

Input/Output Control (IOC): Processes all requests for I/O to be performed on peripheral devices.

Background Tasks:

Job-Control Processor (JCP): Permits the scheduling of VORTEX system or user tasks for background execution. Positions devices to required files, and makes logical-unit and I/O-device assignments.

File-Maintenance Component (FMAIN):

Manages file-name directories and the space allocations of the files. It is scheduled by the JCP upon input of the JCP directive,/FMAIN.

APPENDIX G

PROBE CARD DEVELOPMENT AND THE TAC PROBE UNIT

APPENDIX G

PROBE CARD DEVELOPMENT AND THE TAC PROBE UNIT

A probe card was developed by AFAL to provide an interface between the Singer and the NAND/NOR logic circuit chip shown again in Figure 63. The probe card is shown in Figure 64 under development in the probe card station. A probe is soldered on the probe card corresponding to the contact pad position on the logic gate. The tip of each probe is about 1 mil in diameter and is to make contact with the corresponding pad of the NAND/NOR MESFET circuit of Figures 1 and 2.

The contact pads on the chip of Figure 63 correspond to the connections for the power supply voltages, input/output, and ground provided by the Singer system. Each pad is numbered to correspond with the Singer's matrix pins (Figure 57) of the system performance board. The correspondence of each pad's function with the necessary connections is shown in Table XII. Interface between the performance board and the probe card is provided by low resistive colored ribbon wire and an edge connector receptacle. The probe card is slid into the receptable and in turn is attached to the TAC probe mount as shown in Figure 65.

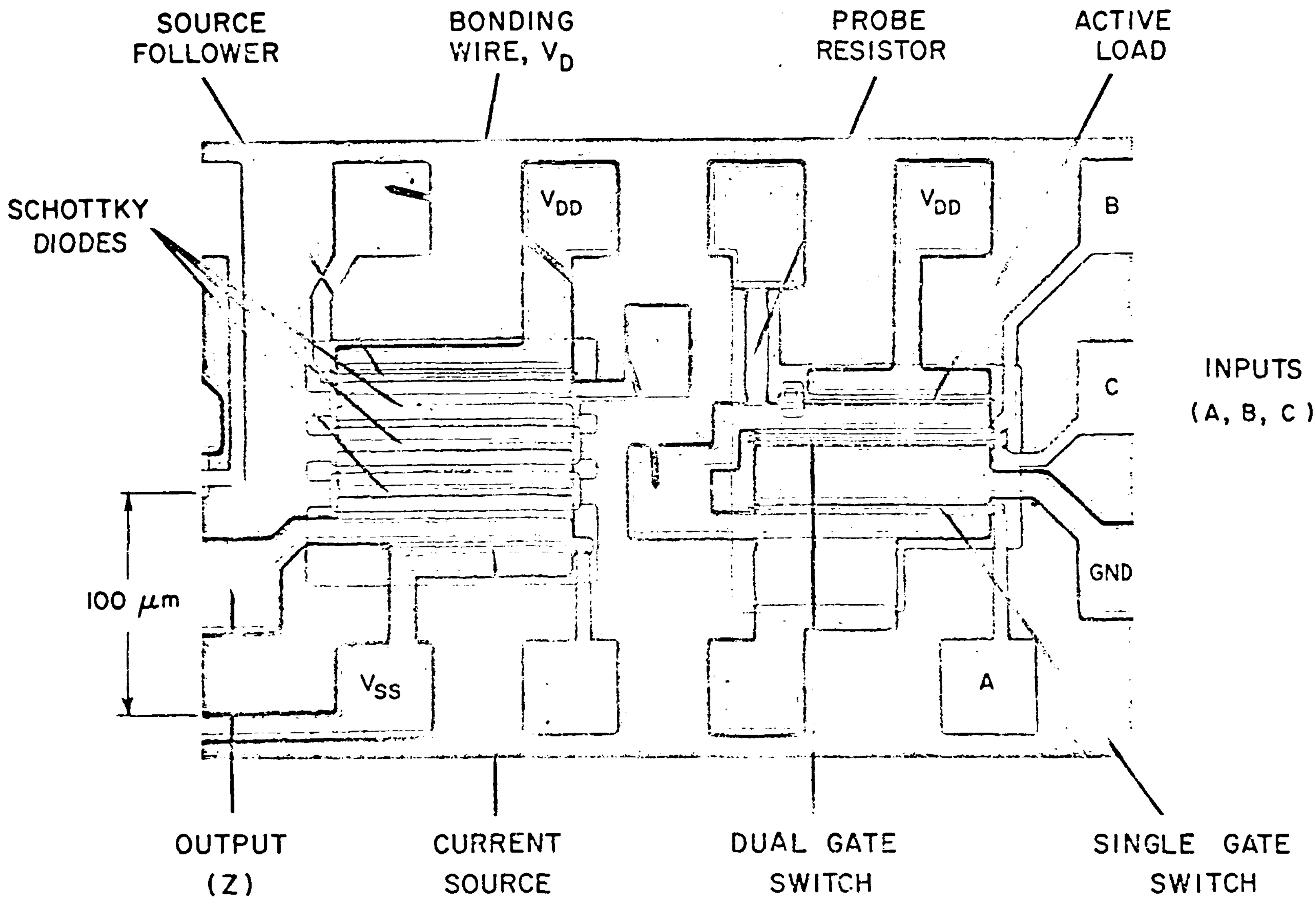
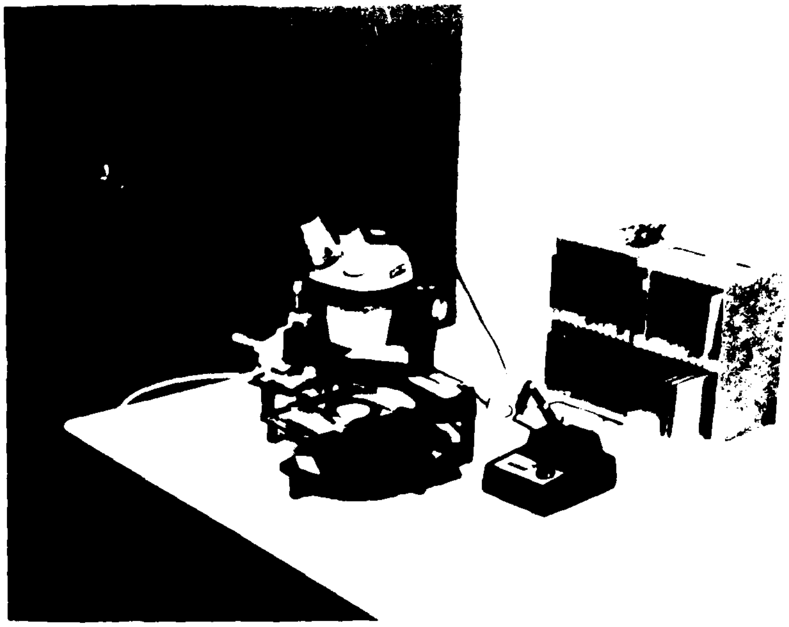


Figure 63. GaAs MESFET Logic Gate Chip.

Table XII. Probe Card Interface Connections.

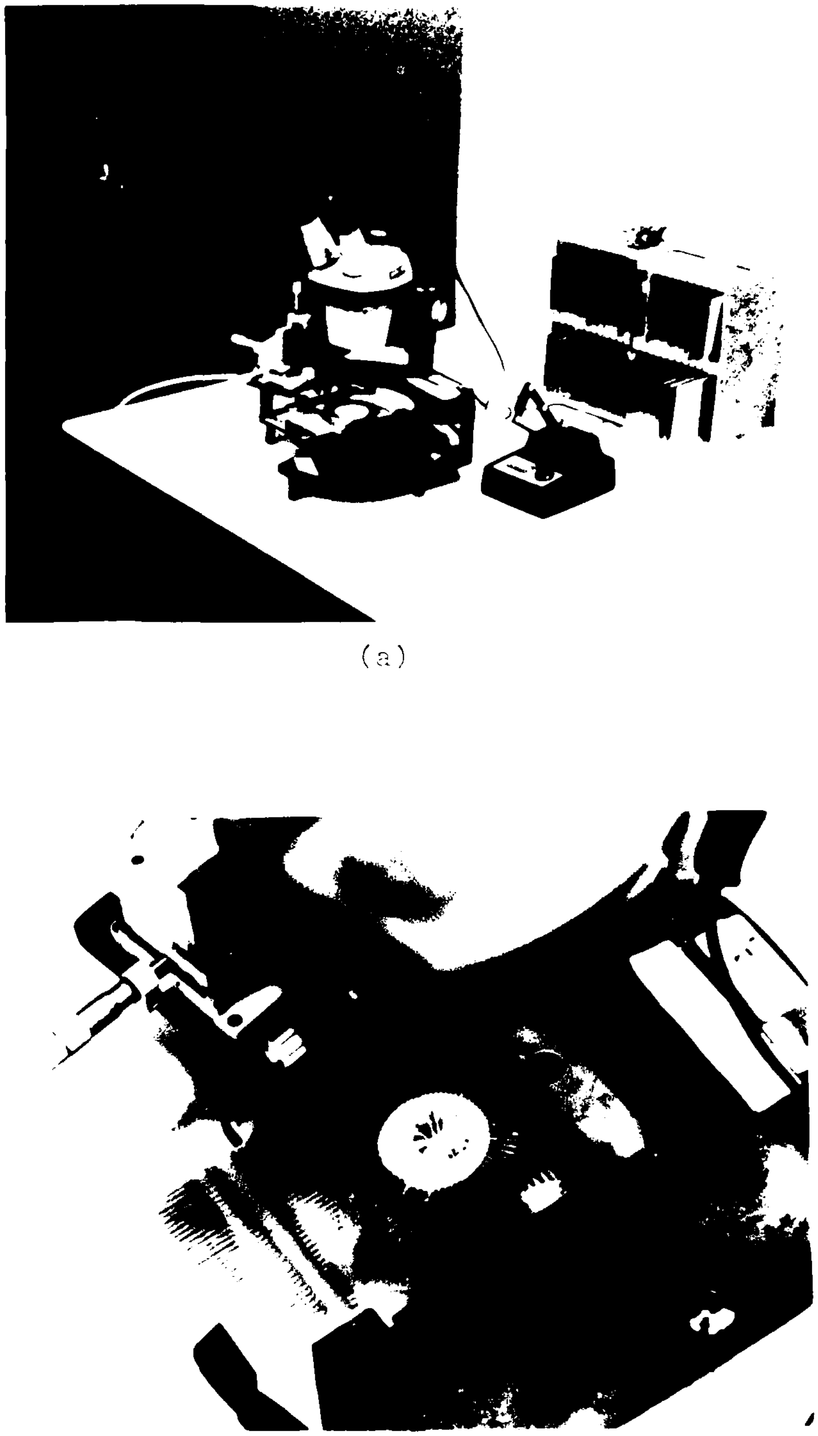
MATRIX PIN NUMBER	WIRE COLOR	EDGE CONNECTOR RECEPTABLE #	PAD FUNCTION
33	RED	B7	ACTIVE LOAD DRAIN (VDD)
34	BROWN	B11	DUAL GATE INPUT B
35	BLACK	B14	DUAL GATE INPUT C
36	WHITE	B17	GROUND
37	GREY	B21	SINGLE GATE INPUT A
38	VIOLET	B26	PROBE RESISTOR
41	BLACK	B29	CURRENT SOURCE GATE
42	WHITE	A31	CURRENT SOURCE SOURCE (VSS)
43	GREY	A28	CURRENT SOURCE DRAIN (Z OUTPUT)
44	VIOLET	A18	SINGLE AND DUAL GATE DRAIN
45	BLUE	A17	SOURCE FOLLOWER SOURCE
46	GREEN	A12	SOURCE FOLLOWER GATE
47	YELLOW	A7	SOURCE FOLLOWER DRAIN (VDD)
48	ORANGE	B1	TEST RESISTOR



(a)

(b)

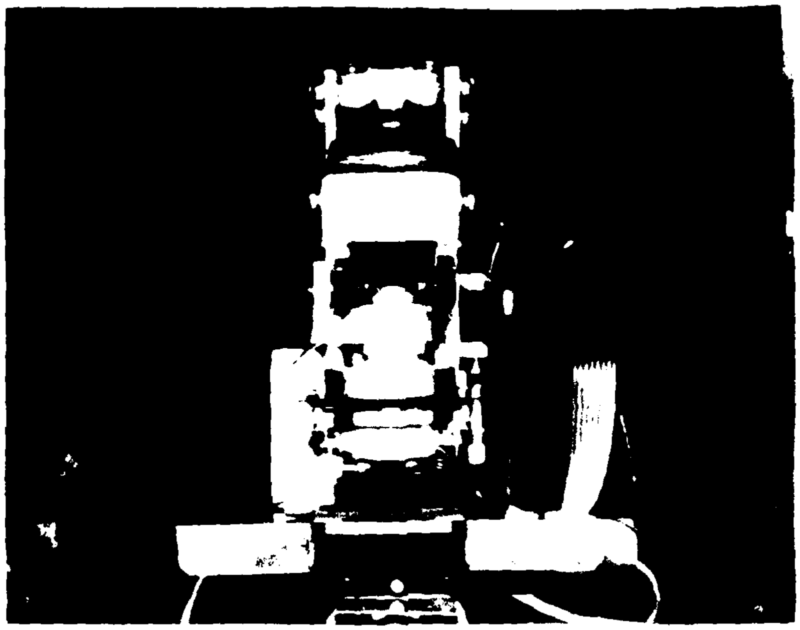
Figure 64. Probe Card Assembly Station. (a) Extended View. (b) Close-Up View.



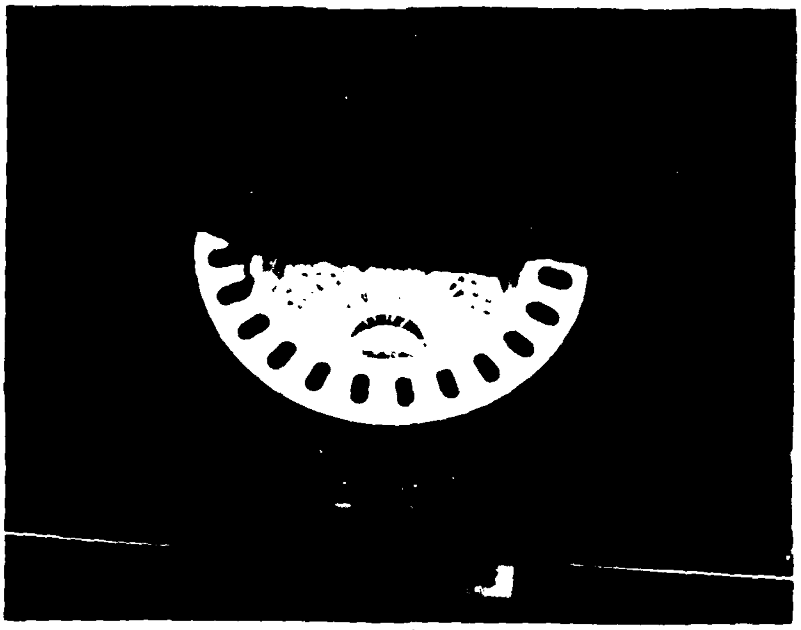
(a)

(b)

Figure 64. Probe Card Assembly Station. (a) Extended View. (b) Close-Up View.



(a)



(b)

APPENDIX H

REQUIRED PROCEDURES TO PERFORM AUTOMATED

TESTING USING THE MESFET PROGRAM

APPENDIX H

REQUIRED PROCEDURES TO PERFORM AUTOMATED TESTING USING THE MESFET PROGRAM

In this appendix, detailed procedures will be presented in order to perform automated testing using the MESFET program. The order of presentation is as follows:

1. Test System Preparation.
2. MESFET Program Usage.
3. MESFET Program Problems.

The programmer is required to understand the procedures in order to run the MESFET program successfully. It should be understood that the MESFET program has not been fully developed due to equipment complications. Areas in the program that may require further investigation will be pointed out. This will reduce any problems that may occur in using the MESFET program to perform automated testing of the GaAs MESFET NAND/NOR logic circuit.

Test System Preparation

In this section, it is assumed that the power supplies, Varian computer, and all peripherals have been turned on prior to performing automated testing. It is also assumed that the power supplies have had at least one hour of warm-up time. Test system preparation will now involve the following (Refer to Figure 66):

1. Load VORTEX operating system into main core memory from the disc using the following:

a. Clear all registers. (Load 0 000 000 000 000 000).

b. Load 0 000 000 000 000 001 into the A register.

c. Load 0 111 111 110 000 000 into the P register.

d. Place VORTEX Boot tape into paper tape/reader punch. Depress LOAD Switch.

e. Press the INT (Interrupt) and Reset switches.

f. Place STEP/RUN switch in RUN position.

g. Press LOAD. The VORTEX Boot tape will now run through the paper tape reader and load the operating system.

h. Loading of the operating system will be indicated by the following address indicated on the register display

0 111 111 110 111 111

i. If the above address is not displayed, the entire process beginning at 'a' must be repeated.

2. Assignment of peripherals will involve determining which peripherals will be used to provide the desired method of I/O:

a. Insure that the CRT, teletype, and line printer are placed 'on-line'.

b. Insure that computer select switch located on back of line printer is set at 'VAR' or Varian.

c. Type; IOLIST on the CRT. The output is as follows:

TE(031) = ECØØ
TA(030) = CTØ3
TL(029) = LPØØ
TO(028) = TYØØ
TI(027) = TYØØ
CO(026) = BCØØ
EO(024) = DØ2B
SE(023) = DØ2A
PL(016) = PØØK
ED(015) = MTØØ
OS(013) = DØØI
ES(014) = DØØJ
SI(002) = CTØØ
SO(003) = CTØØ
PI(004) = CRØØ
LO(005) = LPØØ
BI(006) = PTØØ
BO(007) = PTØØ
SS(008) = DØØ4
GO(009) = DØØG
PO(010) = DØØH
DI(011) = TYØØ
DO(012) = TYØØ
CU(101) = DØØE
SW(102) = DØØF
CL(103) = DØØA
OM(104) = DØØD
BL(105) = DØØC
FL(106) = DØØB

d. If the magnetic tape unit is desired to be used to store or output programs in conjunction with the teletype, type the following on the CRT;

;ASSIGN,TL = TYØØ

;ASSIGN, ED = MTØØ

e. If the magnetic tape unit is desired with the line printer, type the following on the CRT;

;ASSIGN, TL = LPØØ

;ASSIGN, ED = MTØØ

f. To use the line printer in conjunction with the teletype, type the following

;ASSIGN, TL = LPØØ

;ASSIGN, ED = DUM

g. To use the teletype as the primary I/O device, type

;ASSIGN, TL = TYØØ

;ASSIGN, ED = DUM

The teletype can be used to input and store programs regardless of the peripheral assignment. The primary method to input programs is accomplished at procedure 'g'.

3. Scheduling of Tasks will be performed in order to calibrate the test system automatically as well as to begin automated testing:

a. To calibrate the system automatically, insure that procedure '2.f'. is performed.

Then type

;SCHED, CALIB, 2, FL, F

on the CRT. Afterward, refer to the teletype for further instructions. CALIB will indicate the status of all power supplies including sensitivity deviation, offset error, et cetera.

b. To set the system up to perform automated testing, type the following on the CRT:

;SCHED, TEST, 2, FL, F

This completes the preparation of the Singer test system to perform automated testing.

MESFET Program Usage

MESFET program usage will consist of the necessary procedures required to perform tests on the Singer. These procedures are:

a. Refer to Figure 66. Figure 66 indicates the input commands to place into main memory from disc compile, edit, and run the MESFET program.

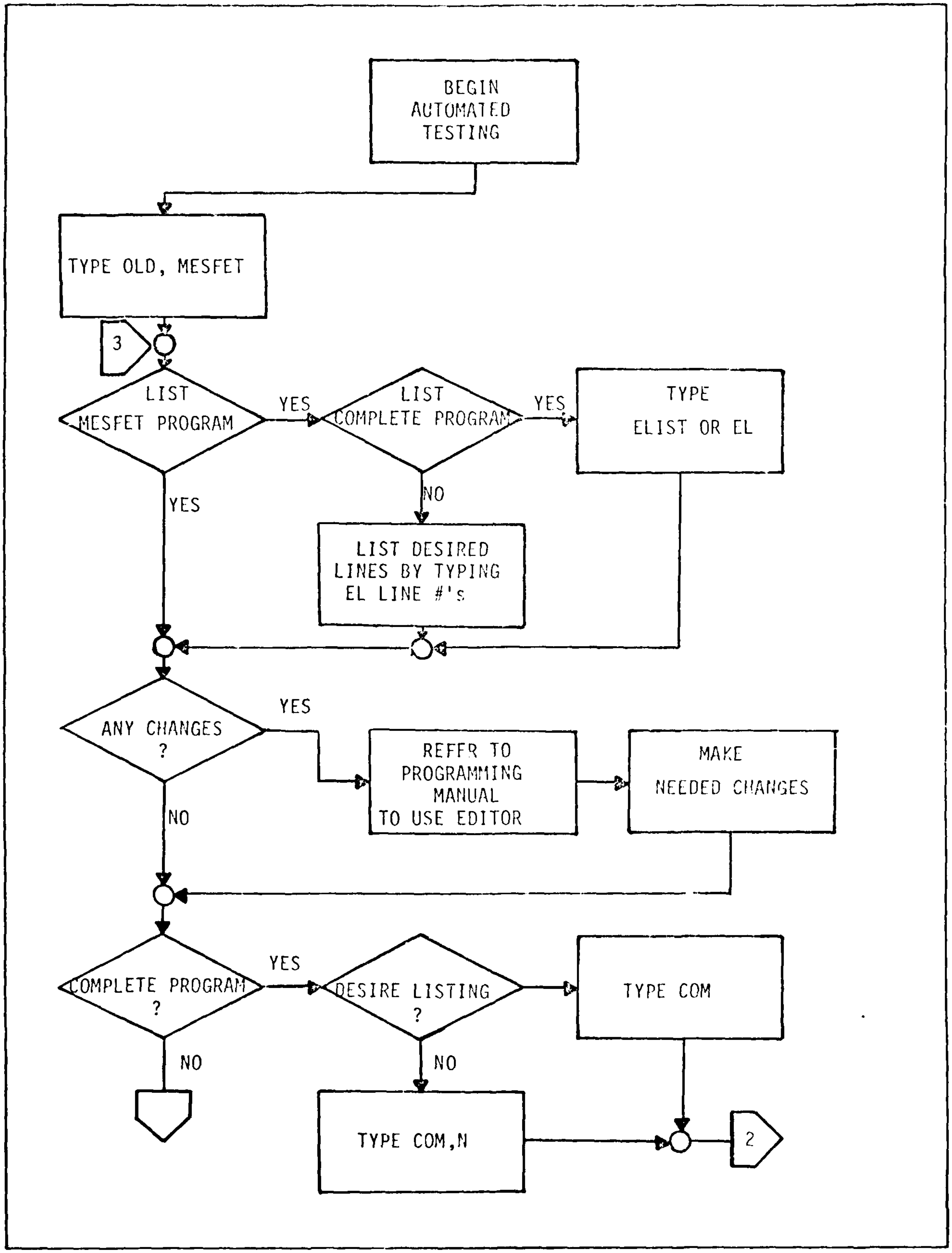


Figure 66. MESFET Program Usage Flowchart.

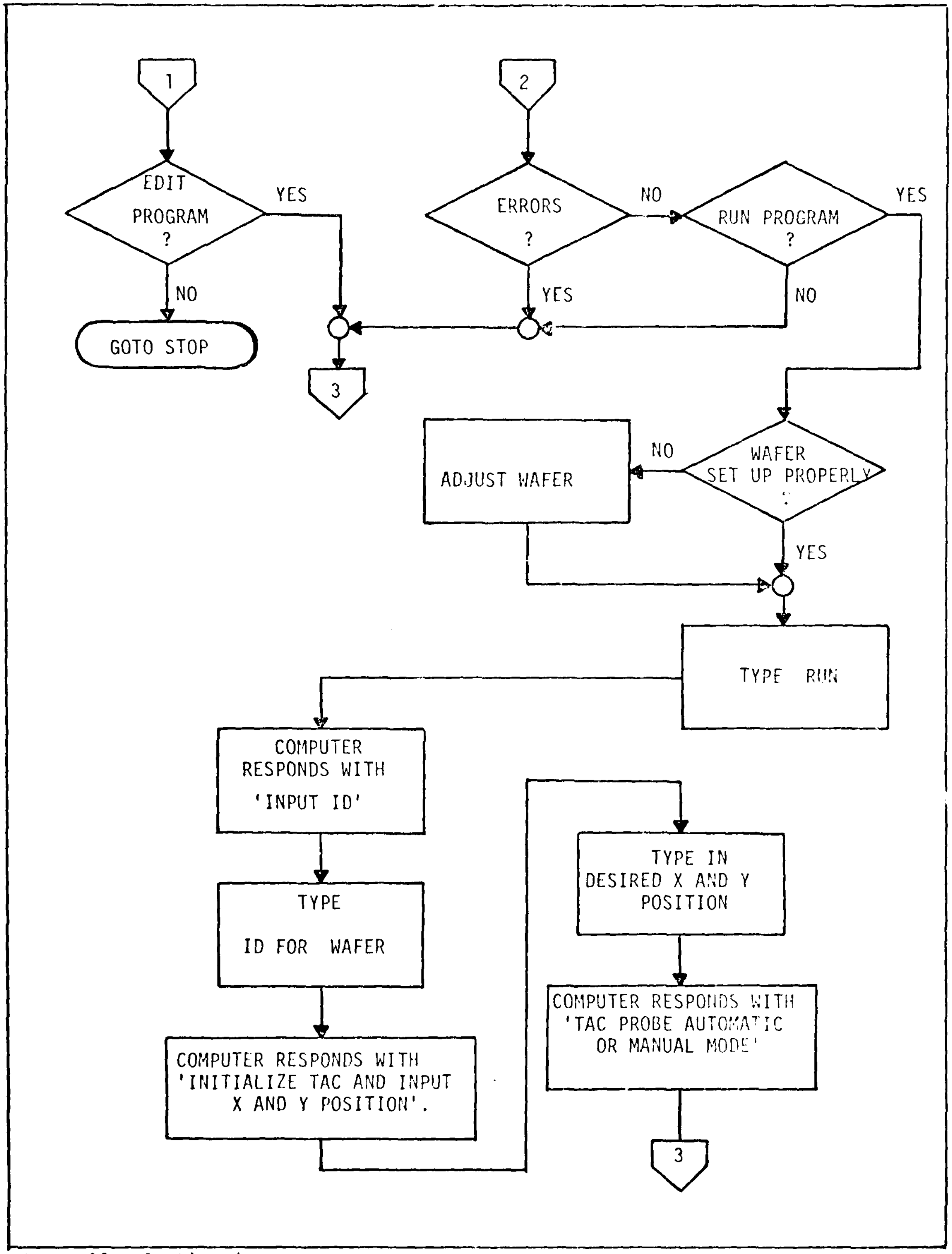


Figure 66. Continued.

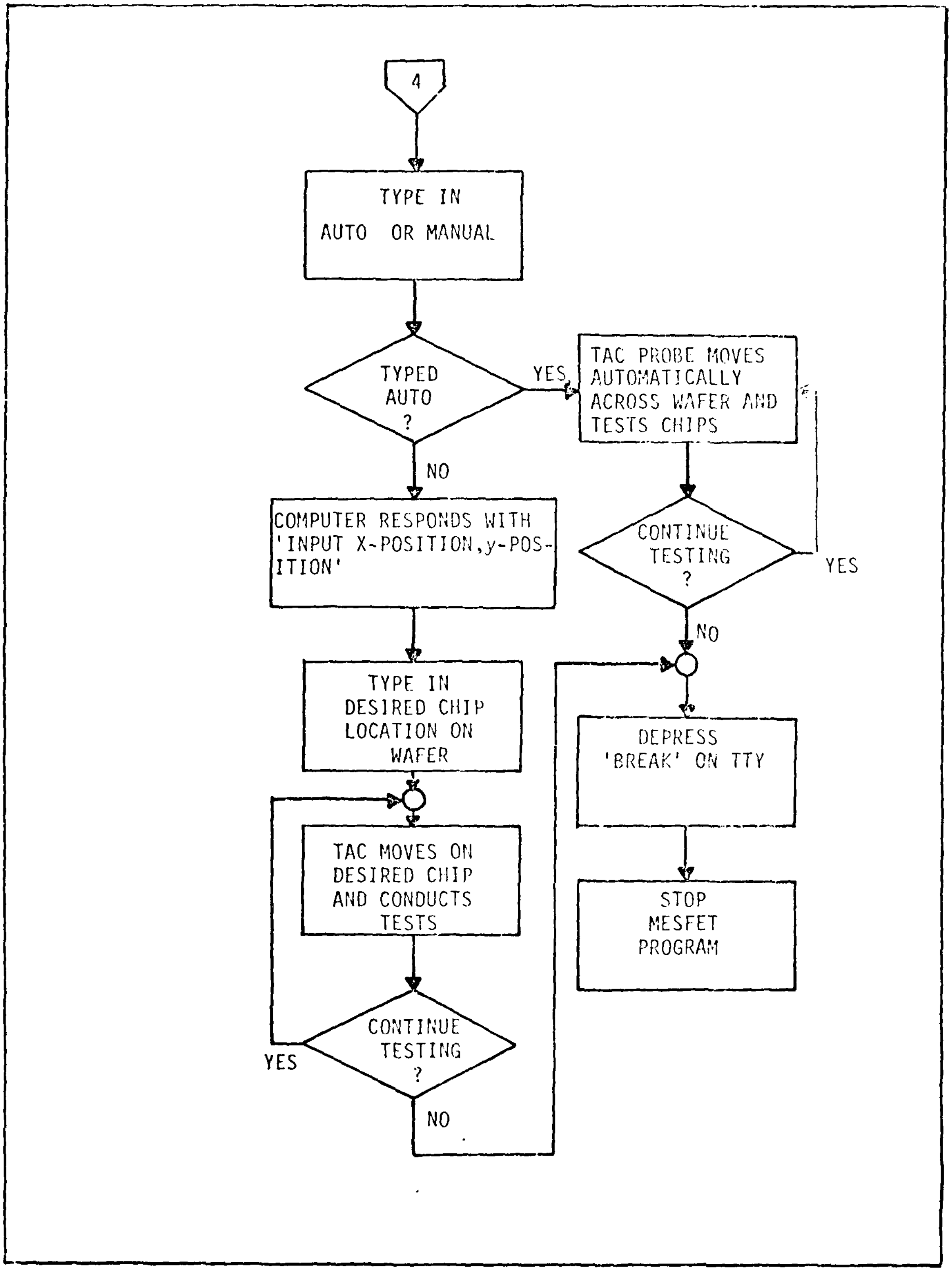


Figure 66. Continued.

b. To store any changes made to the MESFET program type the following:

REPLACE,MESFET

It should be noted that the VARIAN periodically runs into overflow or loses the starting address of the program. This is indicated by the bit overflow display on the VARIAN or that the address display is not lit at all. It is also indicated by no response from the computer on the teletype when RETURN is pressed. All changes made to the program may not be lost. If the previous conditions occur, loading of the operating system is required according to the previously established procedures. Changes made to the program will most likely be kept in the 'scratch' portion of memory where all changes are made prior to storing them on the disc. Generally, there is no need to call the MESFET program to memory the above problems occur.

When calling up the MESFET program, problems may occur, however. These problems are indicated by the fact that the program may not compile correctly as it did before. This is believed to occur when transferring the program from disc to memory. The problem can be minimized by leaving the disc drive and VARIAN on. The program can also be called from main memory (scratch areas) after a period of disuse, but is best to compile the program to determine if any errors do exist. Common errors not noted in the programming manual are:

1. Duplication of lines of code.

3. Omission of code.

If these errors do occur, referral to a correct MESFET program listing is suggested to remove the errors.

APPENDIX I

MESFET PROGRAM

```
350                           :*****/*******************
355                              :**PROGRAM RESET**
360                           :*********************
365   :
370   PRINT 375
375   '                          **PROGRAM RESET**'
380   :
385   PRINT 390
390   '       '
395   PRINT 390
400   :
405                RESET :INITIALIZE THE SINGER TEST SYSTEM
410   :
415                INIT TAC 2 :INITIALIZE THE TAC PROBE USING THE NEXT
416                           :TWO COMMANDS TO DESCRIBE THE NAND/NOR
417                           CIRCUIT'S X-Y DIMENSIONS.
418   :
420                1,20,Y-DIM :ROWS 1-20 AT Y MILS EACH.
425                1,20,Y-DIM :COLUMNS 1-20 AT X MILS EACH.
440   :
441         :**SOURCE-FOLLOWER DC PARAMETER MEASUREMENT**
442   :
445   :
515   PRINT 516
516   '                        **SOURCE-FOLLOWER DC PARAMETER MEASUREMENT**'
517   :
520   :       **SET UP POWER SUPPLIES AND MATRIX SYSTEM**
521   :
525                ENABLE VS1;VS5
530                CLOSE GND;VS1;VS5
535   :
540   :       **PIN ASSIGNMENTS AND INITIAL CONNECTIONS**
541   :
542   :             PIN 47 = DRAIN(VDD)
544   :             PIN 46 = GATE
546   :             PIN 45 = SOURCE
547   :
550                CON GND 46;45;VS5 47
555                CON VMH 47;VML 45
560   :       **DETERMINE DC PARAMETERS OF SOURCE-FOLLOWER**
562   :
565                :**MEASURE IDSS**
570   :
580                SET VS5 5.0V, 20.0MA
585                READ VMH 4
590                PRINT 595 585
595                'VGS=0;VDS='
596   :
600               READ VS5 4  :MEASURE IDSS
605   :
607               MUL,600,1000.0
610               EG,ZS,600
611               EG,ZG,600
```

```
612             FS,ZP,600
615              PRINT 616 TO 617
616             'TOSSET'
617             'TEAT'
620   :
[illegible]             GOSUB 1530 :CALL FG AND RS SUBROUTINE
625   :
627             GOSUB 2600 :CALL LIMITS SUBROUTINE
630   :
[illegible]   :
642   :        PREPARE SINGER TO MEASURE VP
645   :
652             DIS GND 46
657             CON VG1 46
665   :
670             DIS VMF 47
671   :
672             CON VMF 46
680   :
681   :
685             GOSUB 2260 :CALL PINCH-OFF VOLTAGE(VP) SUBROUTINE
690   :
691   :
695             RESET
700   :
701              ENABLE VS1;VS5
705             CLOSE GND;VS1;VS5
710              CON GND 45;VS1 41;VS5 47
715              CON VFF 46;VGL 45
720   :
730   :
735              GOSUB 2840 :CALL TRANSCONDUCTANCE(GM) SUBROUTINE
740   :
741              DIS VS1 46;VFF 46
743              CON GND 46;VFF 47
745   :
750              GOSUB 4215 :CALL BREAKDOWN VOLTAGE(BV) SUBROUTINE
755   :
760   :     **END SOURCE-FOLLOWER DC PARAMETER MEASUREMENT**
765   :
770   PRINT 590
775   PRINT 580
780   :
785              RESET
790   :      **CURRENT SOURCE DC PARAMETER MEASUREMENT**
795   :
800   PRINT 805
805   '      **CURRENT SOURCE DC PARAMETER MEASUREMENT**'
810   :
815   :      **SET UP POWER SUPPLIES AND MATRIX SYSTEM**
820   :
825             ENABLE VS1;VS5
830             CLOSE GND;VS1;VS5
```

```
825  :
830  :     **PIN ASSIGNMENTS AND INITIAL CONNECTIONS**
840  :
845  :           PIN 43 = DRAIN
850  :           PIN 41 = GATE
855  :           PIN 42 = SOURCE
865  :
870         CON GND 42;41;VS5 43
875         CON VMM 43;VML 42
880  :
885  :           **MEASURE IDSS**
890  :
895         SET VS5 5.0V, 20.0MA
900         READ VMM 4
905         PRINT 800 900
908         'VGS=0;VDS='
910  :
912         READ VS5 4 :CALL ID MEASURE SUBROUTINE(MEASURE IDSS)
918          MUL,600,1000.0
920         EQ,25,915
923         EQ,26,915
925         EQ,28,915
930         PRINT 616 25 617
935  :
940  PRINT 350
945  :
950          GOSUB 1330 :CALL RD AND RS MEASUREMENT SUBROUTINE
955  :
958          GOSUB 2000 :CALL LIMITS SUBROUTINE
960  :
966         DIS GND 41
967         CON VS1 41
970          DIS VMM 43
975          CON VMM 41
978  :
980          GOSUB 2260 :CALL PINCH-OFF VOLTAGE(VP) SUBROUTINE
985  :
990          RESET
995  :
1000        ENABLE VS1;VS5
1005        CLOSE GRD;VS1;VS5
1006        CON GND 42;VS1 41;VS5 43
1012        CON VMM 41;VML 42
1015 :
1020        GOSUB 2840  :CALL TRANSCONDUCTANCE(GM) SUBROUTINE
1021 :
1022        DIS VS1 41;VMM 41
1024        CON GND 41;VMM 43
1025 :
1030        GOSUB 4215 :CALL BREAKDOWN VOLTAGE(BV) SUBROUTINE
1035 :
1040 :    **END CURRENT SOURCE DC PARAMETER MEASUREMENT**
1045 :
```

```
1050 PRINT 390
1055 :
1060 :     **ACTIVE LOAD DC PARAMETER MEASUREMENT**
1065 :
1070 PRINT 1075
1075 '        **ACTIVE LOAD DC PARAMETER MEASUREMENT**'
1080 :
1085 :    **SET UP POWER SUPPLIES AND MATRIX SYSTEM**
1090 :
1095            RESET
1100 :
1105            ENABLE VSS
1110            CLOSE GND;VSS
1115 :
1120 :******PIN ASSIGNMENTS AND INITIAL CONNECTIONS*****
1125 :
1130 :            PIN 33 = DRAIN(VDD)
1135 :            PIN 44 = SOURCE
1140 :
1145            CON GND 44;VSS 33
1150            CON VMM 33;VMI 44
1152            SET VSS 5.0V, 20.0MA
1155 :
1160     !***DETERMINE DC PARAMETERS OF ACTIVE LOAD***
1165 :
1170            !**MEASURE IDSS**
1175 :
1180            READ VMM 4
1185            PRINT 555 1180
1188 :
1190            READ VSS 4 !CALL ID MEASURE SUBROUTINE(MEASURE IDSS)
1191            MUL,1190,1000.0
1195            EQ,ZC,1190
1200            EQ,ZA,1190
1205            EQ,ZR,1190
1210            PRINT 616 ZS 617
1211 :
1215 PRINT 390
1220 :
1225            GOSUB 1330 !CALL RD AND RS SUBROUTINE
1230 :
1235            GOSUB 4215 !CALL BREAKDOWN VOLTAGE(BV) SUBROUTINE
1240 :
1245 :    **END ACTIVE LOAD DC PARAMETER MEASUREMENT**
1250 :
1260 PRINT 390
1270 :
1275 :
1290 :    **RD AND RS MEASUREMENT SUBROUTINE**
1295 :
1305 :
1310 GOTO 1950
1315 :
```

```
1330 :
1335           ENTER
1340 :
1345 :           **BEGIN RO MEASUREMENT**
1350 :
1355 :     CALCULATE THE LINEAR ON-RESISTANCE(RO) AT VGS=0 USING THE
1360 :FOLLOWING RELATIONSHIP :
1365 :
1370 :                 RO = VDS2(RO)-VDS1(RO)/ID2(RO)-ID1(RO)
1375 :
1380           SET VSS 2.0V, 20.0MA :**VDS2(RO)**
1385           READ VOM 4           :**MEASURE VDS2(RO)**
1390           EG,7*,1385
1395 :
1400           READ VSS 4           :**ID2(RO)**
1405           EG,76,1400
1410 :
1415           SET VSS 1.0V, 20.0MA :**VDS1(RO)**
1420           READ VOM 4           :**MEASURE VDS1(RO)**
1425           EG,76,1420
1430 :
1435           READ VSS 4           :**ID1(RO)**
1440           EG,26,1435
1445 :
1450 :           **END RO MEASUREMENT**
1455 :
1460 :             **BEGIN RS MEASUREMENT**
1465 :
1470 :     CALCULATE SATURATION RESISTANCE(RS) AT VGS=0 USING THE
1475 :FOLLOWING RELATIONSHIP :
1480 :
1485 :             RS = VDS2(RS)-VDS1(RS)/ID2(RS)-ID1(RS)
1490 :
1495           SET VSS 7.0V, 20.0MA :**VDS2(RS)**
1500           READ VOM 4           :**MEASURE VDS2(RS)**
1505           EG,26,1500
1510 :
1515           READ VSS 4           :**MEASURE ID2(RS)**
1520           EG,71,1515
1525 :
1530           SET VSS 4.0V, 20.0MA :**VDS1(RS)**
1535           READ VOM 4           :**MEASURE VDS1(RS)**
1540           EG,73,1530
1545 :
1550           READ VSS 4           :**MEASURE ID1(RS)**
1555           EG,26,1545
1560 :
1565 GOTO 1760  :PRINT RESISTANCE PARAMETERS MEASURED ABOVE? IF NO,
1570            :LEAVE COMMAND AS IS;IF YES, DELETE COMMAND.
1575 :
1580 PRINT 1585
1585 '   **LINEAR ON-RESISTANCE(RO) OF THE CHANNEL AT VGS=0'
1590 :
```

```
1590          PRINT 1595 ZX 1600
1595          'VDS2(RO)='
1600          'VOLTS'
1605 :
1610          PRINT 1615 ZJ 617
1615          'ID2(RO)='
1620 :
1625          PRINT 1630 ZC 1600
1630          'VDS1(RO)='
1634 :
1640          PRINT 1645 ZG 617
1645          'ID1(RO)='
1650 :
1655 PRINT 1660
1660 '     **SATURATION RESISTANCE(RS) OF THE CHANNEL AT VGS=0**'
1665 :
1670          PRINT 1675 ZF 1600
1675          'VDS2(RS)='
1680 :
1695          PRINT 1700 ZJ 617
1700          'ID2(RS)='
1705 :
1715          PRINT 1720 ZJ 1600
1720          'VDS1(RS)='
1725 :
1730          PRINT 1740 ZK 617
1740          'ID1(RS)='
1745 :
1750 :        **CALCULATE RO**
1755 :
1760          SUB,1365,1420 :**VDS2(RO)-VDS1(RO)**
1765          SUB,Z4,Z0     :**ID2(RO)-ID1(RO)**
1770          DIV,1365,ZE   :**RO=VDS2(RO)-VDS1(RO)/ID2(RO)-ID1(RO)
1771          MUL,1365,1000.0
1775          EQ,ZA,1365
1780 :
1785          PRINT 1790 ZA 1795
1790          'LINEAR ON-RESISTANCE(RO)='
1795          'OHMS'
1805 PRINT 390
1810 :
1815 PRINT 1820
1820 '     **SATURATION RESISTANCE(RS) OF THE CHANNEL AT VGS=0**'
1825 :
1830          SUB,1500,1530 :**VDS2(RS)-VDS1(RS)**
1835          SUB,Z1,ZK :**ID2(RS)-ID1(RS)**
1840          DIV,1500,ZK :**RS=(VDS2(RS)-VDS1(RS))/(ID2(RS)-ID1(RS))**
1841          MUL,1500,1000.0
1845          EQ,ZA,1500
1850 :
1855          PRINT 1860 ZA 1795
1860          'SATURATION RESISTANCE(RS)='
1865 :
```

```
1920 PRINT 590
1925 :
1930            RETURN :RETURN TO MAIN PROGRAM
1935 :
1940 :        **END RD AND RS MEASUREMENT SUBROUTINE**
1945 :
1948 :
1950            NOP      :<<<<<NO OPERATION>>>>>
1970 :
1980 :     **LIMITS SUBROUTINE**
1981 :
1985 GOTO 2210
1990 :
2000            ENTER
2005 :
2010 PRINT 2015
2015 '        **CURRENT LIMITS APPLIED TO DETERMINE VP**'
2020 :
2025 :     VP WILL BE THAT VALUE OF VGS THAT IS REQUIRED TO CAUSE THE
2030 :MEASURED ID TO LIE BETWEEN THE SET LIMITS ACCORDING TO THE
2035 :FOLLOWING :
2040 :
2045 :             0.50% OF IDSS LTE ID LTE 1.5% OF IDSS
2050 :
2055 PRINT 590
2060 :
2065 :              **DETERMINE CURRENT LIMITS**
2066 :
2070            MUL,ZG,0.05      :**ZG=IDSS*0.05**
2075 :
2080            MUL,ZR,0.005      :**ZR=IDSS*0.0050**
2085 :
2090            PRINT 2095 ZR 017 2100
2095            'ZR='
2100            '>>>>>0.50% OF IDSS'
2105 :
2110            PRINT 2115 ZG 017 2120
2115            'ZG='
2120            '>>>>>5.0% OF IDSS'
2121 :
2140 :
2145 PRINT 590
2150 :
2155 :                **DETERMINE VOLTAGE LIMITS**
2160 :
2165 :     THE VGS LIMIT IS AS FOLLOWS :
2170 :
2175 :             VGS=-10.0V LTE "MEASURED VGS" LTE VGS=.0V"
2180 :
2185            RETURN :RETURN TO MAIN PROGRAM
2190 :
2210            NOP     :<<<<<NO OPERATION>>>>>
2220 :
```

```
2250     :******PINCH-OFF VOLTAGE MEASUREMENT SUBROUTINE****
2255 :
2260 GOTO 2270
2270 :
2280              ENTER
2285 :
2315              EQ ,Z9,-6.1V
2320              SET VS1 Z9, 20.0MA
2325 :
2330              READ VSS 4 :<<<<<MEASURE ID>>>>>
2335              EQ,ZZ,2330
2340              MUL,ZZ,ZY
2345 :
2350              READ VMM 4 :<<<<<MEASURE VGS>>>>>
2355 PRINT 2360 2350 2365
2360 '**************************VGS='
2365 '********************'
2370 :
2375 :     DOES THE MEASURED VGS MEET THE CONDITIONS AS SPECIFIED IN
2380 :THE LIMITS SUBROUTINE?
2385 :
2390              DATA IF VMM 2350 -10.0V 0.0V 2430
2395              GOTO 2430
2398 :
2400 :     IF SO, VP MAY NOT HAVE BEEN REACHED YET-THEREFORE, GOTO
2405 :2430. IF NOT, VP CANNOT BE REACHED.
2410 :
2415 :     DOES THE MEASURED ID MEET THE CONDITIONS AS SPECIFIED IN
2420 :THE LIMITS SUBROUTINE?
2425 :
2430              DATA IF ZZ ZR ZR 2590
2431 :
2440 :     WHERE ZR = 0.5% OF IDSS
2445 :           ZR = 1.5% OF IDSS
2450 :           ZS = MEASURED ID
2451 :
2455 :     IF SO, VP HAS BEEN REACHED, THEREFORE, GOTO 2590. IF NOT,
2460 :VP HAS NOT BEEN REACHED YET; THEREFORE CONTINUE.
2470 :
2480 :***********PRINT VGS AND ID AT EACH INCREMENT OF VGS**********
2490 :
2495 PRINT ZR 2496 2505 ZZ 2496 2500 ZS 2490 2510
2496 '=A'
2500 ' LTE'
2505 ' ID='
2510 '?'
2515 :
2520 PRINT 2525
2525 'NO'
2526 :
2527 PRINT 390
2530 GOTO 2340 :<<<<<CONTINUE INCREMENTING VGS AND MEASURING ID>>>>>
2535 :
```

```
2540 PRINT 2545
2545 '***********PINCH-OFF VOLTAGE(VP) CANNOT BE REACHED***********'
2546 :
2550 PRINT 360
2555 :
2560 PRINT 2565 2350
2565 '      VGS='
2566 :
2567 PRINT 2570 2496
2570 '        ID='
2575 :
2580            GOTO 2620 :RETURN TO MAIN PROGRAM
2585 :
2590 PRINT 2595 2350
2595 '     PINCH-OFF VOLTAGE(VP)='
2600 :
2605 PRINT 2610 2496
2610 '                              ID='
2615 :
2620             RETURN :RETURN TO MAIN PROGRAM.
2625 :
2630 :**********************INCREMENT VGS********************
2635 :
2640            ADD,2350,-0.1V
2641            EG,ZP,2350
2645            SET VS1 ZP, 20.0MA
2650 :
2655 GOTO 2330 :CONTINUE MEASURING ID AND VGS.
2660 :*****************END PINCH-OFF(VP) SUBROUTINE***************
2665 :
2670            NOP
2680 :
2805 :
2810            :****TRANSCONDUCTANCE(GM) SUBROUTINE****
2815 :
2820 GOTO 4195
2835 :
2840            ENTER
2845 :
2850 PRINT 2855
2855 '                    **DETERMINE GM**'
2860 :
2925            SET VS5 5.0V, 20.0MA :**VDS=5.0V**
2930 :
2935            SET VS1 0.0V, 20.0MA  :**VGS4=0.0V**
2940            READ VS5 4            :**MEASURE ID4**
2941            EQ,ZL,2940
2945            READ VMH 4            :**MEASURE VGS4**
2950 :
2955            SET VS1 -0.5V, 20.0MA :**VGS3=-0.5V**
2960            READ VS5 4            :**MEASURE ID3**
2961            EQ,ZN,2960
2965            READ VMH 4            :**MEASURE VGS3**
```

```
2970 :
2975             SUB,ZL,ZN            :**ID4-ID3**
2980             SUB,2945,2965        :**VGS4-VGS3**
2985             DIV,ZL,2945          :**GM1=ID4-ID3/VGS4-VGS3**
2990 :
2995             SET VS1 -1.0V, 20.0MA :**VGS=-1.0V**
3000             READ VS5 4            :**MEASURE ID2**
3002             EQ,ZM,3000
3005             READ VM 4            :**MEASURE VGS2**
3010 :
3015             SUB,ZN,ZM            :**ID3-ID2**
3020             SUB,2965,3005        :**VGS3-VGS2**
3025             DIV,ZN,2965          :**GM2=ID3-ID2/VGS3-VGS2**
3030 :
3035             SET VS1 -1.5V, 20.0MA :**VGS=-1.5V**
3040             READ VS5 4            :**MEASURE ID1**
3041             EQ,ZZ,3040
3045             READ VM 4             :**MEASURE VGS1**
3050 :
3055             SUB,ZM,ZZ            :**ID2-ID1**
3060             SUB,3005,3045        :**VGS2-VGS1**
3065             DIV,ZM,3005          :**GM3=ID2-ID1/VGS2-VGS1**
3070 :
3075             ADD,ZL,ZN            :**GM1 + GM2**
3080             ADD,ZL,ZM            :**GM1 + GM2 + GM3**
3085 :
3090 :            **DETERMINE GM**
3095 :
3100             DIV,ZL,3.0           :**GM=(GM1+GM2+GM3)/3.0**
3105 :
3110 :            **TRANSCONDUCTANCE(GM)**
3115 PRINT 3120
3120 '            **TRANSCONDUCTANCE(GM)**'
3125 :
3130 PRINT 3140 ZL 3145
3140 '      GM='
3145 'MILLIMHOS'
3150 :
3155             RETURN :RETURN TO MAIN PROGRAM
3160 :
3165 :      **END TRANSCONDUCTANCE(GM) SUBROUTINE**
4170 :
4180 :
4185             NOP
4200 :
4201 GOTO 4545
4205           :*****BREAKDOWN VOLTAGE(BV) SUBROUTINE****
4210 :
4215             ENTER
4230 :
4235             EQ,ZS,1000.0 :MAXIMUM DIFFERENCE IN SLOPE
4235 :
4240             EQ,ZT,0.0
```

```
4245          EQ,ZF,2.0
4250          EQ,ZV,0.5
4255          EQ,ZC,0.0
4260          EQ,ZM,1.0
4265          EQ,ZG,3.0V
4267 :
4270          SET VS5 ZC, 20.0MA
4271 :
4275          READ VS5 4 :ID1
4280          READ VMH 4 :VDS1
4281 :
4285          ADD,ZC,1.0V :INCREMENT VS5=VDS BY 1.0V
4290          SET VS5 ZC, 20.0MA
4291 :
4295          READ VS5 4
4300          EQ,ZK,4295
4301 :
4305          READ VMH 4
4310          EQ,ZE,4305
4315          EQ,ZM,4305
4316 :
4320          DATA IF ZV ZG ZH 4350 :DETERMINE SLOPE #1 IF ZV=0.5;ELSE
4322                                :DETERMINE NEXT SLOPE IF ZV=2.0
4323 :
4325 :     **DETERMINE NEXT SLOPE
4327 :
4330          SUB,ZA,ZE
4335          SUB,ZJ,ZK
4340          DIV,ZA,ZJ
4342 :
4347 :
4350          DATA IF ZF ZG ZH 4400 :IINCREMENT VS5=VDS BY 0.5V IF
4352                                :ZF=2.0; ELSE DETERMINE SLOPE #1
4354                                :IF ZF=0.5.
4355 :
4360          SUB,4305,4295
4361 :
4365 :     **DETERMINE SLOPE #1**
4370 :
4375          SUB,4305,4280
4380          SUB,4295,4275
4385          DIV,4305,4295
4390          EQ,ZM,4305
4395 :
4400          ADD,ZC,1.0V :INCREMENT VS5=VDS BY 1.0V
4405          SET VS5 ZC, 20.0MA
4410 :
4415          READ VS5 4
4420          EQ,ZJ,4415
4422 :
4425          READ VMH 4
4430          EQ,ZI,4425
4435          EQ,ZA,4425
```

```
4440            EQ,ZT,4425
4442 :
4445 :     **DETERMINE NEXT SLOPE**
4447 :
4450            SUB,ZI,ZE
4455            SUB,ZJ,ZK
4460            DIV,ZI,ZJ
4465            SUB,ZI,ZP
4467 :
4470            DATA IF ZI ZT ZS 4515 :IS DIFFERENCE IN TWO MEASURED
4472                                  :SLOPES LESS THAN OR EQUAL TO
4474                                  :1000.0 ? IF SO, BV HAS NOT BEEN
4476                                  :REACHED YET. THEREFORE, INCREMENT
4478                                  :VS5=VDS BY 1.0V AND CONTINUE. IF
4480                                  :NOT, THE SLOPE DIFFERENCE IS
4482                                  :GREATER THAN 1000.0. THEREFORE,
4484                                  :BV HAS BEEN REACHED.
4485 :
4490 PRINT 4495 ZS
4495 'BREAKDOWN VOLTAGE(BV)='
4501 :
4505            GOTO 4535 :RETURN TO MAIN PROGRAM
4510 :
4515            EQ,ZV,2.0
4520 :
4525            GOTO 4285 :INCREMENT VS5=VDS BY 1.0V.
4530 :
4535            RETURN :RETURN TO MAIN PROGRAM.
4540 :
4545            NOP
4550 :
4555 :         **SINGLE GATE A(SGA) AND DUAL GATE B,C(DGB,DGC) DC**
4557 :                   **PARAMETER MEASUREMENT**
4565            RESET
4570 :
4575 :     **SET UP POWER SUPPLIES AND MATRIX SYSTEM**
4576 :
4580            ENABLE VS1;VS2;VS5
4585            CLOSE GND;VS1;VS2;VS5
4590 :
4595 :     **PIN ASSIGNMENTS AND INITIAL CONNECTIONS**
4596 :
4600 :            PIN 34 = INPUT B (DGB >> GATE)
4605 :            PIN 35 = INPUT C (DGC >> GATE)
4610 :            PIN 36 = GND (SOURCE)
4615 :            PIN 37 = INPUT A (SGA >> GATE)
4620 :            PIN 44 = DRAIN
4625 :
4630            CON GND 36;37;VS2 34;35;VS5 44
4635            CON VRH 44;VRL 36
4640 :
4645            SET VS5 5.0V, 20.0MA :APPLY 5.0V TO DRAIN
4650 :
```

```
4665           SET VS2 -5.0V, 20.0MA :ASSURE VP=-5.0V FOR DGB AND DGC.
4670 :
4675           READ VMH 4 :VDS AT VGS=0.0V
4680 :
4685           READ VSS 4 :MEASURE IDSS FOR SGA
4686           MUL,4685,1000.0
4687           EQ,ZS,4685
4688           EQ,ZN,4685
4689           EQ,ZR,4685
4690 :
4695 :     **DETERMINE VP OF SGA**
4700 :
4705           GOSUB 2000 :CALL LIMITS SUBROUTINE
4710 :
4715           DIS GND 37
4720           DIS VMH 44
4725           CON VMH 37
4730           CON VS1 37
4735 :
4736 PRINT 4737
4737 '              MEASURE VP OF SGA'
4738 :
4740           GOSUB 2260 :CALL VP SUBROUTINE TO MEASURE VP OF SGA
4745 :
4750           EQ,Z0,2335 :SET Z0 EQUAL TO VP
4755 :
4760           DIS VS2 34;35;VS1 37
4765           CON VS2 37
4770 :
4775           SET VS2 Z0, 20.0MA :LEAVE SGA AT VP.
4780 :
4785           CON GND 34
4787           DIS VMH 37
4790           CON VMH 44
4791 :
4792 PRINT 4793
4793 '          MEASURE DUAL GATE B(DGB) DC PARAMETERS'
4794 :
4795 :     **BEGIN DUAL GATE B(DGB) DC PARAMETER MEASUREMENT**
4796 :
4800           READ VSS 4 :MEASURE IDSS FOR DUAL GATE B(DGB)
4805           MUL,4800,1000.0
4810           EQ,ZS,4800
4815           EQ,ZN,4800
4820           EQ,ZR,4800
4821 :
4825           PRINT 616 ZS 617 :PRINT IDSS OF DGB.
4830 :
4835           GOSUB 1330 :CALL RD AND RS SUBROUTINE
4840 :
4845           GOSUB 2000 :CALL LIMITS SUBROUTINE
4850 :
4855           DIS GND 34
```

```
4860          CON VS1 34
4861          DIS VMH 44
4865          CON VMH 34
4870 :
4875          GOSUB 2280 :CALL VP SUBROUTINE
4876 :
4880          EQ,ZJ,2335
4885 :
4890          GOSUB 2840 :CALL TRANSCONDUCTANCE(GM) SUBROUTINE
4895 :
4900          DIS VS1 34;VMH 34
4905          CON GND 34;VMH 44
4910 :
4915          GOSUB 4215 :CALL BV SUBROUTINE
4920 :
4925 :     **END DUAL GATE B(DGB) DC PARAMETER MEASUREMENT**
4930 :
4935 :     **BEGIN DUAL GATE C(DGC) DC PARAMETER MEASUREMENT**
4940 :
4945          DIS GND 34
4950          CON GND 35
4955 :
4960          READ VSS 4 :MEASURE IDSS FOR DUAL GATE C(DGC)
4965          MUL,4960,1000,9
4970          EQ,ZS,4960
4975          EQ,ZD,4960
4980          EQ,ZR,4960
4985 :
4990          GOSUB 1330 :CALL RD AND RS SUBROUTINE
4995 :
5000          GOSUB 2000 :CALL LIMITS SUBROUTINE
5005 :
5010          DIS GND 35
5015          CON VS1 35
5020          DIS VMH 44
5025          CON VMH 35
5030 :
5035          GOSUB 2280 :CALL VP SUBROUTINE
5040 :
5045          EQ,ZP,2335 :SET ZP EQUAL TO VP OF DGC
5050 :
5055          GOSUB 2840 :CALL GM SUBROUTINE
5060 :
5065          DIS VS1 35;VMH 35
5070          CON GND 35;VMH 44
5075 :
5080          GOSUB 4215 :CALL BV SUBROUTINE
5085 :
5090 :     **END DUAL GATE C(DGC) DC PARAMETER MEASUREMENT**
5095 :
5100 :     **BEGIN SINGLE GATE A(SGA) DC PARAMETER MEASUREMENT**
5105 :
5110          RESET
```

```
5115 :
5120 :     **SET UP POWER SUPPLIES AND MATRIX SYSTEM**
5125 :
5130           ENABLE VS1;VS2;VS5
5135           CLOSE GND;VS1;VS2;VS3;VS5
5140 :
5145 :          **INITIAL CONNECTIONS**
5150 :
5155           CON GND 36;VS1 37;VS2 34;VS3 35;VS5 44
5156           CON VMH 37;VML 36
5165 :
5170           SET VS2 7J, 20.0MA :SET DPH AT VP
5175           SET VS3 ZF, 20.0MA :SET DSL AT VP
5180           SET VS5 5.0V, 20.0MA :APPLY 5.0V TO DRAIN
5185 :
5190           PRINT 015 4665 017 :PRINT IDSS FOR SINGLE GATE A(SGA)
5195 :
5200           GOSUB 2000 :CALL RG AND RS SUBROUTINE
5205 :
5210           GOSUB 2640 :CALL GC SUBROUTINE
5215 :
5220           DIS VS1 37;VMH 37
5225           CON GND 37;VMH 44
5230 :
5235           GOSUB 4215 :CALL BV SUBROUTINE
5240 :
5245 :     **END SINGLE GATE A(SGA) DC PARAMETER MEASUREMENT**
5250 :
5255 :     **BEGIN DIODE DC PARAMETER MEASUREMENT**
5260 :
5262           RESET
5263 :
5265 :     **SET UP POWER SUPPLIES AND MATRIX SYSTEM**
5270 :
5275           ENABLE VS5
5280           CLOSE GND;VS5
5285 :
5290 :     **PIN ASSIGNMENTS AND INITIAL CONNECTIONS**
5295 :
5300 :           PIN 45 = ANODE(A)
5305 :           PIN 43 = CATHODE(C)
5310 :
5315           CON GND 43;VS5 45
5320           CON VMH 45;VML 43
5325 :
5330 PRINT 5335
5335 '     SCHOTTKY DIODES' FORWARD THRESHOLD VOLTAGE(VF) MEASUREMENT'
5340 :
5345 :     **BEGIN SCHOTTKY DIODES' FORWARD THRESHOLD VOLTAGE(VF)**
5350 :                          **MEASUREMENT**
5355           E0,Z5,1.0V
5360           SET VS5 Z5, 20.0MA
5365 :
```

```
5370            READ VFM 4 :MEASURE VOLTAGE
5375            PRINT 5380 5370
5380            '      V='
5385 :
5390            READ VSS 4 :MEASURE CURRENT
5395            PRINT 5400 5390
5400            '      I='
5405 :
5410            DATA IF VSS 5390 0.5MA 1.0MA 5460 :IS MEASURED CURRENT
5415                                              :WITHIN THE INDICATED
5420                                              :LIMITS ? IF SO, VF
5425                                              :HAS BEEN REACHED. IF
5430                                              :NOT, CONTINUE INCRE-
5435                                              :MENTING VSS BY 1.0V.
5440 :
5445            ADD,ZS,1.0V
5450            GOTO 5360
5455 :
5460            PRINT 5465 5370
5465            '      VF='
5470 :
5475            PRINT 5480 5375
5480            'I = VF='
5485 :
5490 :     **END SCHOTTKY DIODES' FORWARD THRESHOLD VOLTAGE(VF)**
5495 :                          **MEASUREMENT**
5500 :
5505 PRINT 5510
5510 '     SCHOTTKY DIODES' REVERSE THRESHOLD VOLTAGE(VR) MEASUREMENT'
5515 :
5520 :     **BEGIN SCHOTTKY DIODES' REVERSE THRESHOLD VOLTAGE(VR)**
5525 :                            **MEASUREMENT**
5530 :
5535            RESET
5540 :
5545 :     **SET UP POWER SUPPLIES AND MATRIX SYSTEM**
5550 :
5555            ENABLE VSS
5560            CLOSE GND;VSS
5565 :
5570 :     **INITIAL CONDITIONS**
5575 :
5580            CON GND 45;VSS 46
5585            CON VFM 46;VFL 45
5590 :
5595            EQU,ZS,1.0V
5600            SET VSS ZS, 20.0MA
5605 :
5610            READ VFM 4 :MEASURE VOLTAGE
5615            PRINT 5380 5610
5620 :
5625            READ VSS 4 :MEASURE CURRENT
5630            PRINT 5400 5625
```

```
5635 :
5640        DATA IF VSS 5625 -1.0MA -2.0MA 5695 :IS THE MEASURED
5645                                           :CURRENT WITHIN THE
5650                                           :INDICATED LIMITS ?
5655                                           :IF SO, VR HAS BEEN
5660                                           :REACHED. IF NOT,
5665                                           :CONTINUE INCREMEN-
5670                                           :TING VSS BY 1.0V.
5675 :
5680        ADD,ZS,1.0V
5685        GOTO 5560
5690 :
5695        PRINT 5405 5610
5700 :
5705        PRINT 5480 5625
5710 :
5715 :  **END SCHOTTKY DIODES' REVERSE THRESHOLD VOLTAGE(VR)
5720 :                   **MEASUREMENT**
5725 :
5800 :       **BEGIN RESISTANCE MEASUREMENT**
5805 :
5810       RESET
5815 :
5820 :       **INITIAL CONNECTIONS**
5825 :
5830        CON RAH 44;RAL 46
5835 :
5840 :       **MEASURE TEST RESISTOR**
5845 :
5850        READ RAH 4 ;READ OHMMETER
5855        PRINT 5860 5850
5860        'TEST RESISTOR='
5865 :
5870        RESET
5875 :
5880 :       **INITIAL CONNECTIONS**
5885 :
5890        CON RAH 44;RAL 36
5895 :
5900 :       **MEASURE PROBE RESISTOR**
5905 :
5910        READ RAH 4 ;READ OHMMETER
5915        PRINT 5920 5910
5920        'PROBE RESISTOR='
5925 :
5930        INDEX TAC 5950 :IF ALL CHIPS IN THE SPECIFIED ARRAY HAVE
5935                       :BEEN TESTED, GOTO LINE 5955. IF NOT,
5940                       :GOTO LINE 515 AND CONTINUE TESTING.
5945        GOTO 515
5950 :
5955        PRINT 5960
5960        'DONE WITH ARRAY'
5965 :
5970        END :END OF MESFET PROGRAM.
```

APPENDIX J

FOUR-BIT ACCUMULATOR TEST RESULTS

AND CONCLUSIONS

APPENDIX J

FOUR-BIT AFIT/AFAL ACCUMULATOR TEST RESULTS AND CONCLUSIONS

The objective of the work to follow is to present the procedures, obtain results, and draw conclusions from the automated testing of the 4-bit AFIT/AFAL accumulator chip, Figures 67 and 68. The accumulator was designed and developed by the Microprocessor Design course (EE 6.95/6.96) students at AFIT in the Spring and Summer Quarters of 1978. The advisor and teacher for this effort was Major J. M. Borky. The accumulator was developed and finally fabricated using the AFIT and AADE integrated circuit fabrication facilities. The Singer tester was used to perform the testing of the accumulator.

Design Operation of the 4-Bit Accumulator

Referring to Figure 67, the accumulator accepts 4 data inputs (DBØ-DB3) with a total of 2^4 or 16 combinations as shown in Table XIII. The accomulator is to perform the following data operations: parallel load, shift left, shift right, rotate, and nothing. Control signals CACCØ, CACC1, and CACC2 control the operations which are listed in Table XIV.

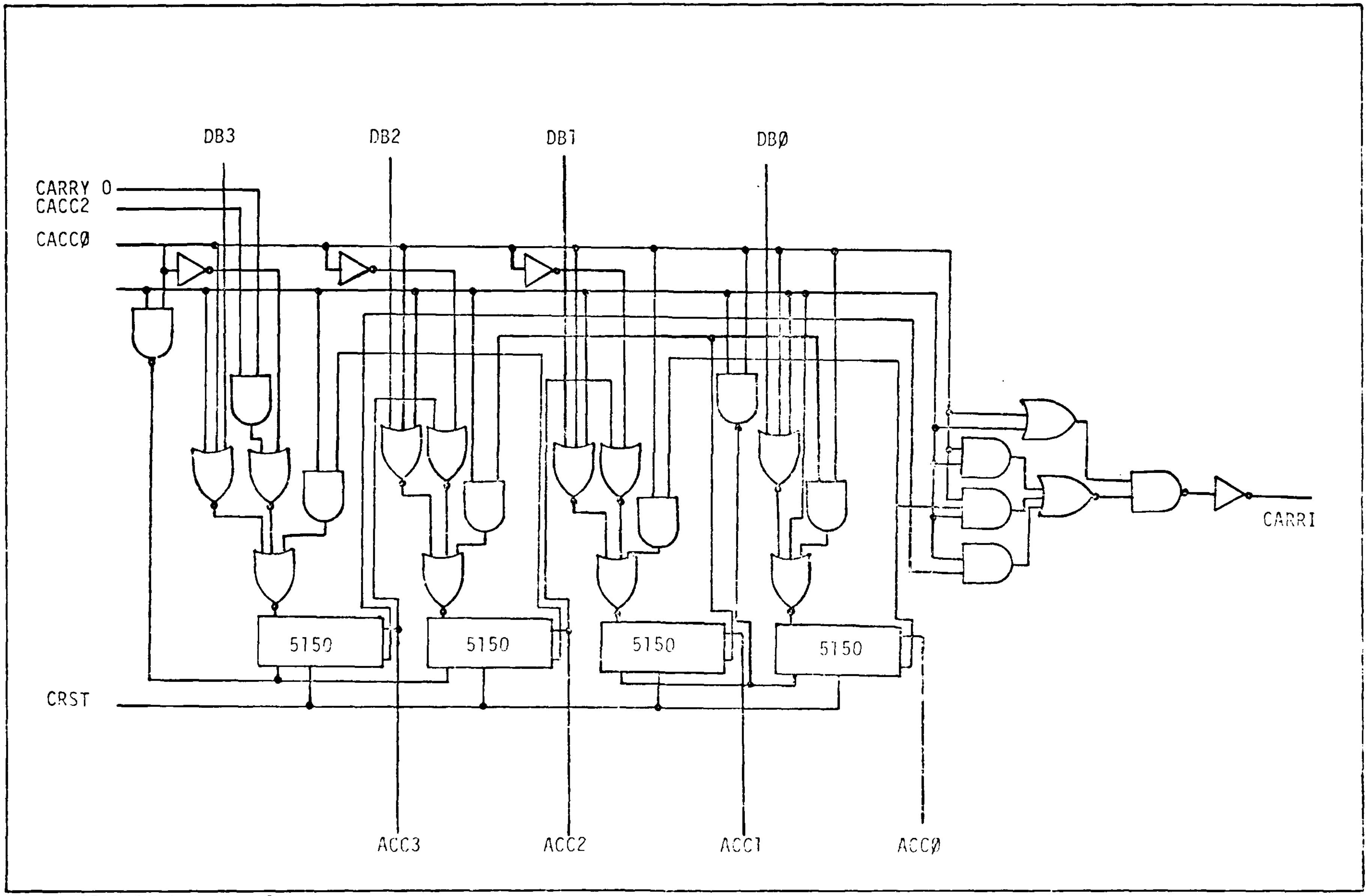


Figure 67. 4-Bit Accumulator.

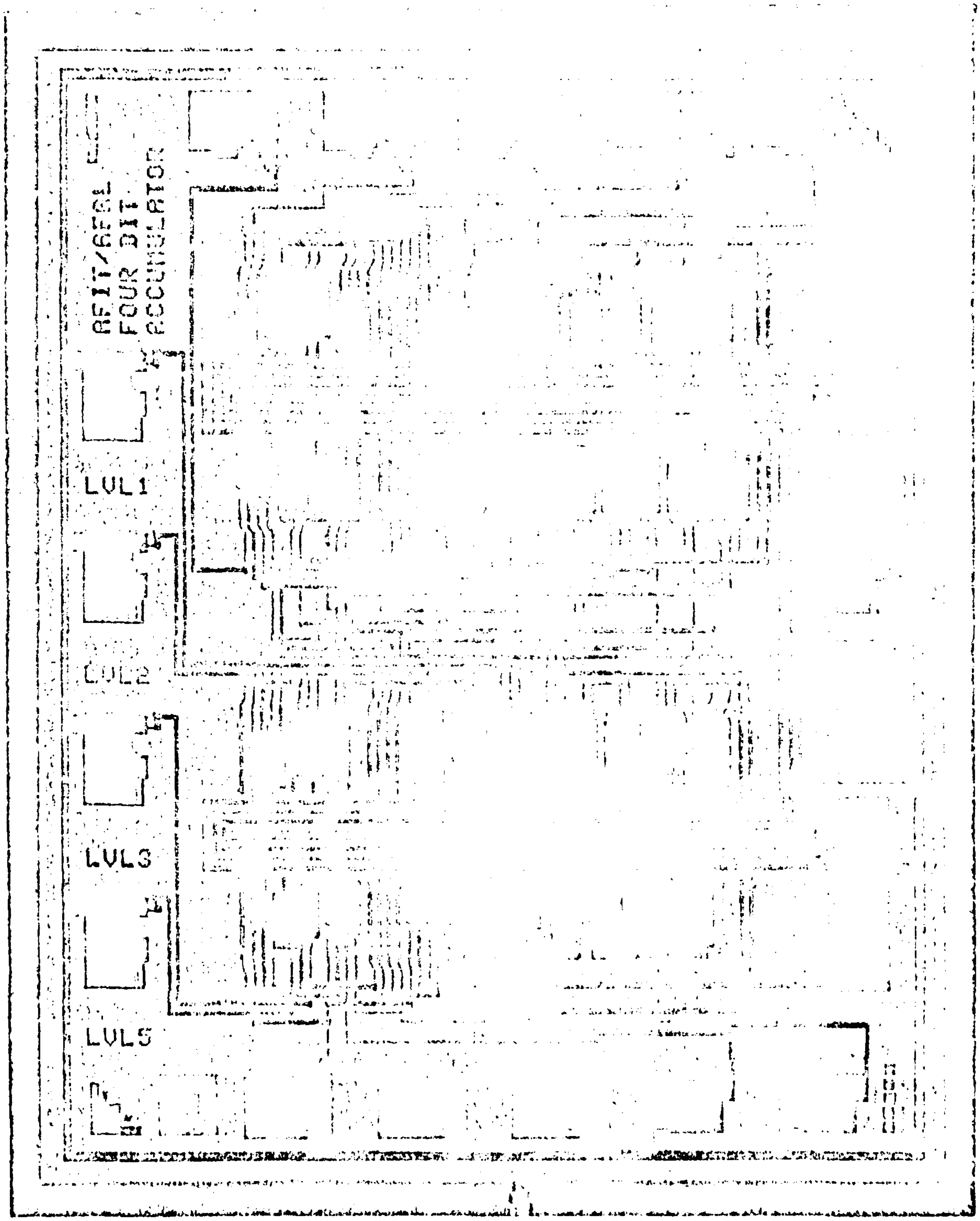


Figure 68. 4-Bit Accumulator Chip.

Table XIII. 4-Bit Accumulator Input Data.

DB3	DB2	DB1	DBØ
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

The accumulator was designed and developed using silicon gate P-MOS transistors. The use of P-MOS devices requires the use of negative logic inputs. The accumulator also requires two phase clock signals, ϕ_x and ϕ_y, to transfer the data (DBØ-DB3) to the outputs ACC⌀-ACC3 according to the appropriate set of control signals. The gate requires two biases: V_{dd} at -7.0V and V_{gg} at -14.5V. A reset control signal, CRST, is included to reset the accumulator to zero. Since negative logic is used, a logic 1 is set at -7.0 and a logic 0 at, 0.0V or ground potential. These inputs and their appropriate logic levels are listed in Table XV. The timing diagram of Figure 69 indicates the relationship of control to phase clock signals to be used to shift data. The designers of the accumulator design the device to shift data after ϕ_x,ϕ_y phase clocks were applied to the device.

Automated Testing of the 4-bit Accumulator

A means was needed to test the 4-bit accumulator after its fabrication at AFWAL/AADE. The Singer tester was a logical choice to test the accumulator at the wafer level. In order to test the device, a probe card was required to be developed to interface the device with the Singer tester. The probe card was inserted into the TAC probe unit just as in the testing of the MESFET. Table XVI lists the functions of the bonding pads and the assigned probe card pin numbers.

Automated Testing Procedures. Now that the functions of the various signals have been noted, it is now time to state the testing procedures used to determine the performance of the 4-bit accumulator. The following is a simple algorithm adopted for one particular testing procedure for the Singer tester:

1. Reset the Singer tester.
2. Set up the appropriate power supplies.
3. Input desired data.
4. Apply desired control signals to either parallel load, shift left, shift right, or rotate the deisred data.
5. Apply ϕ_x, ϕ_y.
6. Stop.

The above algorithm was implemented into a program to be used on the Singer Tester.

Automated Testing Results and Conclusions. The objective of the testing of the 4-bit accumulator was to determine if it was capable of performing the data operations as indicated in Table XIV. The little known fact in the testing of the 4-bit accumulator was that of the clock rates that were required to transfer data to the outputs ACCØ-ACC#. This was not available in the provided documentation nor from a consultation with one of the designers of the accumulator. From Chapter VI, it was noted that the highest frequency available on the Singer was about 62.5 Hz. Consultation with the advisor indicated that the clock rates required for the accumulator were somewhat higher. As a result, no valid data was obtained from the accumulator testing. The main problem experimented in using the Singer was that the clock rates and therefore the period and pulse widths of the control signals could not be controlled. Given the fact that these characteristics were unknown, made it even more difficult to provide the proper signal characteristics required by the Singer. The source code was not capable of providing the proper signal characteristics required by the accumulator whatever they were. The source code provides mainly for static testing only and is limited to the testing of DC parameters. A further study of this area is presented in Chapter VI.

In conclusion, the Singer tester is not capable of providing variable clock rates to the degree of flexibility required by some circuits. From the testing it was discovered that the source code was also not capable of providing the clock pulses ϕ_x, ϕ_y as in Figure 69 due to the fact mentioned above. ϕ_x would simply overlap ϕ_y. The automated testing of the 4-bit accumulator served as a basic exercise to understand the Elucidate testing language and testing techniques, the Singer tester itself and its capabilities. This experience aided in the development of the automated testing programs to test the GaAs MESFETs of Figure 19.

Table XIV. 4-Bit Accumulator
Control Signals.

CACCO	CACC1	CACC2	FUNCTION
0	0	--	PARALLEL LOAD
0	1	--	SHIFT LEFT
1	0	0	SHIFT RIGHT
1	0	1	ROTATE
1	1	--	NOTHING

Table XV. 4-Bit Accumulator
Voltage Inputs.

VOLTAGE INPUTS	HIGH	LOW
CACCØ-CACC2	-7.0	0.0
DBØ-DB3	-7.0	0.0
CRST(RESET)	-7.0	0.0
V_{DO}	-7.0	0.0
V_{GG}	-7.0	0.0
$Ø_x$	-7.0	0.0
$Ø_y$	-7.0	0.0
CARRØ	-7.0	

Table XVI. 4-Bit Accumulator Probe Card Interface Connections.

BONDING PAD FUNCTION	PIN NUMBER
ACC1	1
ACC2	2
DB2	3
CARRI	4
DB1	5
RESET	6
DBØ	7
CACC2	8
CARRYØ	9
CACCØ	11
DB3	10
CACC1	14
ACC3	13
ACCØ	12
V_{GG}	15
ϕ_x	16
GND	17
V_{DD}	18
ϕ_y	19
V_{GG}	20

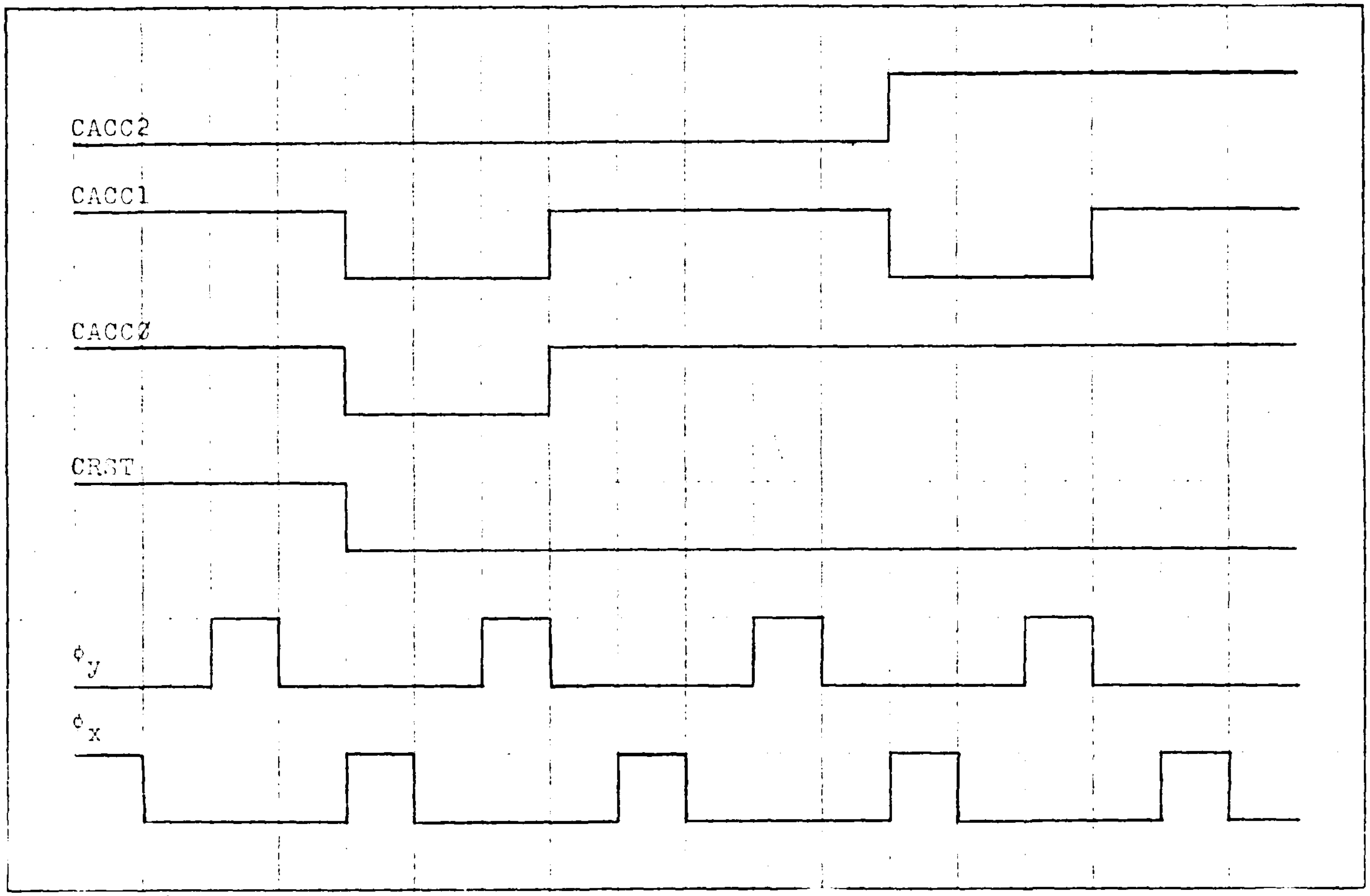


Figure 69. Timing Diagram Showing Relationship of Control Signals to Phase Clocks.

Automated Testing Procedures. Now that the functions of the various signals have been noted, it is now time to state the testing procedures used to determine the performance of the 4-bit accumulator. The following is a simple algorithm adopted for one particular testing procedure for the Singer tester:

1. Reset the Singer tester.
2. Set up the appropriate power supplies.
3. Input desired data.
4. Apply desired control signals to either parallel load, shift left, shift right, or rotate the desired data.
5. Apply ϕ_x, ϕ_y.
6. Stop.

The above algorithm was implemented into a program to be used on the Singer Tester.

Automated Testing Results and Conclusions. The objective of the testing of the 4-bit accumulator was to determine if it was capable of performing the data operations as indicated in Table XIV. The little known fact in the testing of the 4-bit accumulator was that of the clock rates that were required to transfer data to the outputs ACCØ-ACC3. This was not available in the provided documentation nor from a consultation with one of the designers of the accumulator. From Chapter VI, it was noted that the highest frequency available on the Singer was about 62.5 Hz. Consultation with the advisor indicated that the clock rates required for the accumulator were somewhat higher. As a result, no valid data was obtained from the accumulator testing. The main problem experienced in using the Singer was that the clock rates and therefore the period and pulse widths of the control signals could not be controlled. Given the fact that these characteristics were unknown, made it even more difficult to provide the proper signal characteristics required by the Singer. The source code was not capable of providing the proper signal characteristics required by the accumulator whatever they were. The source code provides mainly for static testing only and is limited to the testing of DC parameters. A further study of this area is presented in Chapter VI.

In conclusion, the Singer tester is not capable of providing variable clock rates to the degree of flexibility required by some circuits. From the testing it was discovered that the source code was also not capable of providing the clock pulses ϕ_x, $_y$ as in Figure 69 due to the fact mentioned above. ϕ_x would simply overlap ϕ_y. The automated testing of the 4-bit accumulator served as a basic exercise to understand the Elucidate testing language and testing techniques, the Singer tester itself and its capabilities. This experience aided in the development of the automated testing programs to test the GaAs MESFETs of Figure 19.

APPENDIX K

SINGLE GATE DC PARAMETER MODEL DATA

TABLE XVII DC Parameter Data For Source Follower Characteristic Curves, Figure 14.

I_{DSS}(mA) = 11.6

V_p(V) = 08.0

g_m(mmho) = 2.2

R_d(ohm) = 3.0

V_{DS}(V)	V_{GS}(v)	R_o(Ohm)	R_s(Ohm)	I_D(mA) CALC.	I_D(mA) MEAS.	REGION
0.0	0.0	184	2500	0.0	0.0	
0.5				2.71	3.2	
0.0				5.84	6.0	LINEAR
1.5				8.1	8.4	
2.0				10.8	10.3	
2.5	0.0	184	2500	11.7	11.5	
3.0				11.96	11.9	
3.5				12.1	12.0	SAT
4.0				12.33	12.3	
4.5				12.52	12.5	
5.0				12.7	12.6	
0.0	-1.0	229	2500	0	0	
0.5				2.18	2.8	
1.0				4.80	5.2	LINEAR
1.5				6.55	7.2	
2.0				8.73	8.8	
2.5	-1.0	229	2500	9.04	9.4	
3.0				9.22	9.6	
3.5				9.40	9.8	SAT
4.0				9.69	10.0	
4.5				9.77	10.2	
5.0				9.95	10.4	
0.0	-2.0	294	1785	0.0	0.0	
0.5				1.7	2.4	
1.0				4.0	4.4	LINEAR
1.5				5.1	5.8	
2.0	-2.0	294	1785	6.55	6.5	
2.5				6.79	6.9	
3.0				7.03	7.2	
3.5				7.27	7.5	SAT
4.0				7.51	7.6	
4.5				7.75	8.0	
5.0				7.99	8.2	

V_{DS}(V)	V_{GS}(V)	R_o(Ohm)	R_s(Ohm)	I_D(mA) CALC.	I_D(mA) MEAS.	REGION
0.0 0.5 1.0	-3.0	416	2500	0.0 1.2 2.7	0.0 1.8 3.0	SAT
1.5 2.0 2.5 3.0 3.5	-3.0	416	2500	4.1 1.5 4.73 4.90 5.0	3.8 4.4 4.6 4.8 5.1	SAT
4.0 4.5 5.0				5.25 5.4 5.59	5.2 5.6 5.7	SAT
0.0 0.5 1.0 1.5	-4.0	675	2500	0.0 0.8 1.6 2.3	0.0 0.8 1.6 2.0	
2.0 2.5 3.0 3.5 4.0 4.5 5.0				2.7 2.9 3.1 3.2 3.40 3.65 3.80	2.4 2.6 2.8 3.0 3.2 3.4 3.6	
0.0 0.5 1.0 1.5 2.0	-5.0	1250	2500	0.0 0.4 0.8 1.2 1.5	0.0 0.4 0.8 1.1 1.2	LINEAR
2.5 3.0 3.5 4.0 4.5 5.0	-5.0	1250	2500	1.75 1.88 2.00 2.15 2.28 2.42	1.4 1.59 1.7 1.9 2.0 2.2	SAT
0.0 0.5 1.0	-6.0	2500	2500	0.0 0.2 0.4	0.0 0.2 0.4	LINEAR

V_{DS}(V)	V_{GS}(V)	R_o(Ohm)	R_S(Ohm)	I_D(mA) CALC.	I_D(mA) MEAS.	REGION
1.5	-6.0	2500	2500	0.66	0.70	
2.0				0.76	0.80	
2.5				0.86	0.82	
3.0				0.96	0.98	SAT
3.5				1.05	1.10	
4.0				1.16	1.20	
4.5				1.26	1.22	
5.0				1.36	1.40	
0.0	-7.0	5000	2500	0.0	0.0	
0.5				0.1	0.2	LINEAR
1.0				0.2	0.22	
1.5				0.26	0.30	
2.0				0.33	0.40	
2.5				0.39	0.42	
3.0				0.46	0.46	
3.5				0.52	0.70	SAT
4.0				0.59	0.80	
4.5				0.66	0.81	
5.0				0.73	0.82	
0.0	-8.0	10000	2500	0.0	0.0	
0.5				0.05	0.1	LINEAR
1.0				0.1	0.15	
1.5	-8.0	10000	2500	0.12	0.2	
2.0				0.16	0.21	
2.5				0.24	0.39	
3.0				0.26	0.40	SAT
3.5				0.28	0.41	
4.0				0.319	0.42	
4.5				0.36	0.44	
5.0				0.40	0.46	

APPENDIX L

ALTERNATE METHOD TO RESOLVE CURRENT

MEASURING INACCURACY OF THE SINGER TESTER

APPENDIX L

ALTERNATE METHOD TO RESOLVE CURRENT MEASURING INACCURACY OF THE SINGER TESTER

The purpose of this appendix is to present a method used to attempt to resolve the current measuring inaccuracy of the Singer tester. According to the results presented in Chapter V, MESFET drain currents were inaccurate by as much as 1.1mA. An inaccuracy such as this value prevented the MESFET program to determine the pinch-off voltage of a MESFET. Comparisons between curve tracer photographs (I-V characteristics) and the results obtained with the Singer were made to determine that a problem with the tester truly existed. To verify this problem, a simple program to measure resistance was written and implemented on the Singer as follows:

```
100  RESET
110  ENABLE VS5
120  CLOSE GND; VS5
130  CON GND 40; VS5 35
140  SET VS5 5.0V, 100.0mA
150  CON VMH 35; VML 40
160  READ VS5 4
170  READ VMH 4
180  PRINT 190 160
190  'I='
200  PRINT 210 170
210  'V='
```

```
220  PAUSE    :    PROGRAM HALTS UNTIL PROGRAMMER
230                INSTRUCTS PROGRAM TO CONTINUE.
240  PRINT 250
250  '    '
260  GOTO 160:     MEASURE NEXT RESISTANCE VALUE.
270  END
```

A decade resistance box was connected across pins 35 and 40 of the performance board. The resistance was increased by 1,000 ohms when the program halted each time at line 220 above. The maximum resistance set on the decade box was 50,000 ohms. The voltage was set at 5.0V with current measured at each value of resistance. The actual current was calculated using ohms at each value of resistance. Experimental currents were measured on the Singer for each value of resistance. The results obtained and the error factors are shown in Table XVIII for values of resistance between 5,000 and 50,000 ohms at 5,000 ohm increments. The error factors were calculated by dividing calculated values of current by the measured values.

Table XVIII Current Measuring Accuracy of the Singer

RESISTANCE(Ohms)	CALCULATED CURRENT(mA)	MEASURED CURRENT(mA)	ERROR FACTOR
5000	1.00	1.86	0.53
10000	0.50	1.35	0.37
15000	0.33	1.35	0.37
20000	0.25	1.12	0.22
25000	0.20	1.08	0.18
30000	0.17	0.02	0.17
35000	0.14	1.01	01.3
40000	0.12	0.99	0.12
45000	0.11	0.98	0.11
5000	0.10	0.96	0.10

Error factors for currents for resistances between 1,000 and 50,000 ohms were obtained but not shown in the table. A mean error factor value was then obtained for several values of current throughout the resistance range. The MESFET program was then set up to multiply a drain current by the appropriate error factor when the measured current was within the current range for the specified error factor.

Using the above method to obtain the proper drain currents did not prove fruitful. The objective was to develop a simple method to resolve the current measuring inaccuracy of the Singer as discussed in Chapter V. Solving this problem would hopefully provide the capability to obtain pinch-off using the MESFET program since current measuring accuracy is important.

Another but similar method was then attempted to resolve the current accuracy problem. Without going into detail, curve tracer I-V characteristics (Figure 70) were obtained for a SOURCE FOLLOWER MESFET. The same MESFET was then tested on the Singer to determine experimental values of drain current (Table XX). Error factors were determined for values of current as shown in Table XIX.

Table XIX. Error Factors Used to Resolve Current Measuring Inaccuracy of the Singer.

CURRENT RANGE (mA)	ERROR FACTOR
4.0 to 8.5	0.84
3.0 to 3.9	0.74
2.25 to 2.9	0.64
1.70 to 2.24	0.54
1.45 to 1.69	0.45
1.27 to 1.44	0.38
1.20 to 1.26	0.30

Cont.

Table XIX Continued.

CURRENT RANGE (mA)	ERROR FACTOR
1.15 to 1.19	0.25
1.11 to 1.14	0.22
1.07 to 1.10	0.12
1.01 to 1.06	0.10
0.05 to 1.00	0.05
0.00 to 0.04	0.01

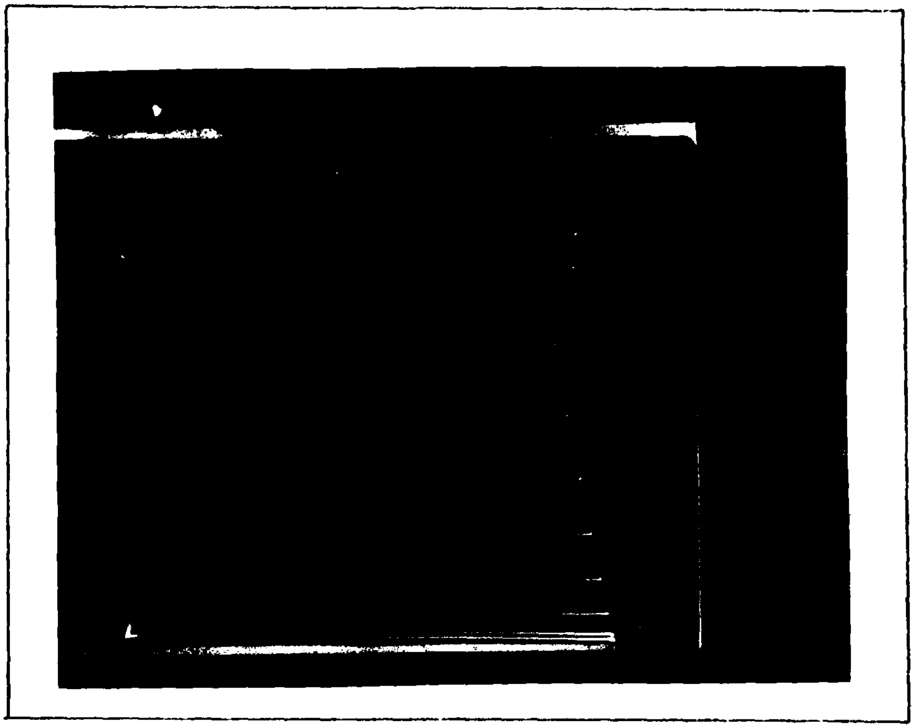


Figure 70. Sample MESFET Used to Obtain Error Factors.

Table XX . Error Factor Results for a SOURCE FOLLOWER.

DC PARAMETER	CURVE TRACER	SINGER	SINGER*
VDS(V)	5.0	4.99	4.99
IDSS(mA)	3.7	4.94	4.10
VP(V)	-1.6	1.59	-1.59
ID(mA)	0.01	1.15	0.05
LIMITS	VP@ 0.27% of IDSS	0.5%<ID<1.5%	
VGS(V)	ID(mA)	ID(mA)	ID(mA)
-1.0	0.56	1.75	0.96
-1.2	0.25	1.40	0.54
-1.4	0.05	1.21	0.[illegible]7
-1.6	0.01	----	----

VITA

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REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER AFIT/EE/GE/80- 7	2. GOVT ACCESSION NO. AD-A100 762	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) The Automated DC Parameter Testing of GaAs MESFETs Using the Singer Automatic Integrated Circuit Test System		5. TYPE OF REPORT & PERIOD COVERED MS THESIS 6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) THOMAS L. HARPER 1st Lt USAF		8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS Air Force Institute of Technology (AFIT-EN) Wright-Patterson AFB, Ohio 45433		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS		12. REPORT DATE Sept 1980 13. NUMBER OF PAGES 232
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) AFWAL/AADE Wright-Patterson AFB OH		15. SECURITY CLASS. (of this report) UNCLASSIFIED 15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

Approved for public release; IAW AFR 190-17

Frederic C. Lynch

FREDERIC C. LYNCH, Major, USAF
Director of Public Affairs

16 JUN 1981

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

GaAs MESFETs
GaAs
MESFETs
Automated Testing
DC Parameter Testing
GaAs MESFET DC Modeling

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Procedures, in the form of a computer program, were developed to automate the manual testing of the DC parameters of GaAs MESFETs, integrated resistors, and Schottky diodes. These devices are elements of a NAND/NOR logic circuit developed by Hewlett-Packard. The Singer Automatic Integrated Circuit Test System located at the Air Force Wright Aeronautical Laboratories, Avionics Laboratory, Microelectronics Branch (AFWAL/AADE), Wright-Patterson AFB OH, was used to develop these procedures.

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The following DC parameters for the above devices were to be tested using the Singer tester: drain-to-source voltage (V_{DS}), saturated drain current (I_{DSS}) at gate-to-source voltage (V_{GS}) at 0.0 volts, pinch-off voltage (V_P), transconductance (g_m), breakdown voltage (BV) at V_{GS} = 0.0 volts, diode forward and reverse threshold voltages, and resistance. Procedures have been written to test all of these parameters with actual test results obtained for the following MESFET parameters: V_{DS}, I_{DSS}, V_{GS}, linear on-resistance and saturation resistance, V_P and g_m. Unfortunately, due to system measurement accuracies, these results do not compare favorably when compared with curve tracer I-V curves of the MESFETs. This report will attempt to demonstrate the feasibility of the Singer to test these parameters given the status of the system.

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